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D06-先进微电子与光电子材料
D06-Advanced Microelectronic and Optoelectronic Materials

主办单位

中国材料研究学会

会议网址: https://cmc2025.scimeeting.cn

D06. 先进微电子与光电子材料

分会主席：赵超、俞文杰、杨德仁

邀请报告

D06-01

半导体相变存储器

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智慧城市、5G、物联网、云计算、人工智能等 “大数据”的兴起对计算机架构提出了更高的要求，从冯诺依曼架构发展到存算一体架构是必然趋势。相变存储器（PCRAM）具有非易失、微缩性能好、与 CMOS 工艺兼容、循环寿命长、高速读取、可三维集成等优点，被认为是最具潜力的下一代非挥发存储技术。PCRAM 可以填补 DRAM 与 FLASH 之间的性能鸿沟，解决目前计算机机架构中“存储墙”的问题，也可以作为神经形态芯片实现类脑计算，将会在数据中心、汽车电子、物联网和人工智能等方面获得大规模应用。报告介绍了课题组近年来在相变存储器研究方面的进展，包括相变材料可逆相变机理、高速相变材料、高性能开关材料与机理，相变存储器产业化进展等。

D06-02

基于 28/22nm CMOS 平台的 RRAM 工艺模块和宏单元

钱鹤

清华大学

开发了基于 28/22nm CMOS Foundry 的阻变存储器（RRAM）工艺模块和相应的宏单元，包括 material stack 优化、器件侧壁保护、初始低阻（ILR）消除、宏单元设计技术和通过操控算法优化存储特性等，获得了良好的 macro IP 性能，非常适合 MCU、smart card、DDIC 及其它需要 eNVM 的 SoC 应用，也非常适合存算一体（CIM）芯片的应用。

D06-03

高性能铪基铁电存储器

吕杭柄

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铪基铁电存储器凭借优异的可微缩性和工艺兼容性、接近 DRAM 的读写时延以及良好的非易失性，成为下一代高密度，低功耗，高性能存储芯片的核心候选技术。但目前该技术面临铁电极化物理起源不明晰、可靠性不满足大规模商业应用需求的难题，亟需从底层机理探索性能优化路径。本报告涵盖铪基铁电材料相变动力学、器件可靠性和技术应用等多个方

面。在材料机理方面，通过球差电镜对退火过程和后道工艺热预算下的材料相结构进行原位表征，首次观测到铁电相以四方相为母相，从氧空位富集区形核扩展的过程及后道工艺温度下四方相和铁电相的可逆相变过程，阐明了铁电相形成及后道热预算下的性能退化机理。在器件可靠性方面，通过结构和电学表征，提出高电场不可逆铁电-单斜相变和低场可逆铁电-pbca 相变的双疲劳机制模型，并同步建立了铪基铁电存储器在保持、耐久及间隔读等多可靠性场景下的电学模型。在技术应用层面，结合机理研究成果，成功研制出基于 40nm CMOS 工艺的 32Mb 嵌入式 3D FeRAM 芯片。该芯片在 125℃下耐久性超 1e13 次，保持特性达 10 年，展现了铪基铁电存储技术在存储密度和性能上的巨大潜力。

D06-04

闪存存储器在 AI 时代的关键技术路径

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在人工智能（AI）技术迅猛发展的背景下，全球对算力与存力的需求持续攀升，传统二维平面存储架构难以满足 AI 大模型训练、边缘计算等场景对高密度存储与高效存算协同的严苛要求，这一需求驱动产业界积极布局超大容量高密度存储技术，存储技术也实现从二维平面到三维垂直架构的跨越式发展，其中 3D NAND 闪存凭借其立体堆叠优势，迅速成为大容量非易失存储器市场的主流选择。与此同时，基于三维架构的存内计算等新型存储技术不断突破，为打破"内存墙"瓶颈、实现算力存力协同进化提供了创新路径。然而，三维架构在提升存储密度的同时，也带来了前所未有的可靠性挑战，其多层堆叠工艺、垂直阵列架构以及存算融合场景下的特性需求，使其退化机制和可靠性优化策略呈现高度复杂性。为构建面向 AI 时代的高可靠存储体系，亟需建立从介质物理特性到系统架构的全栈协同优化方法论。本报告将阐述基于闪存介质底层特性的可靠性优化策略，分析闪存在存算协同技术中的应用潜力，展望三维存储芯片未来发展的关键技术路径。

D06-05

自旋存储材料与器件技术

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自旋电子技术是利用电子本征自旋属性实现非易失信息存储，具有低功耗、高速度、高密度、抗辐照等优势特性，有望突破传统 CMOS 工艺的功耗瓶颈，支撑物联网、人工智能等新兴应用的快速发展。结合非易失存储与可重构逻辑运算功能，自旋存储器 MRAM 可进一步集成构建“存算一体”架构，为解决 “冯诺依曼架构瓶颈”问题提供有效途径。本报告将从功能材料生长、物理机制探索、器件结构优化、芯片研发等方面介绍自旋存储材料与器件

最新科研进展并进行展望。

D06-06

忆阻器计算技术

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人类社会正在由信息化时代迈向智能化时代。在这一过程中，边缘人工智能（AI）的应用逐步增多，涵盖了科研、医疗、交通和生活等多个领域。然而，如何在计算资源受限的边缘设备中，实现更丰富的 AI 功能成为当前面临的一个关键挑战。忆阻器是指器件的电阻在外电场作用下可以被调节至多个不同的电阻状态，并且对调节过程具备一定记忆能力的器件。通过构建大规模忆阻器阵列，并结合相应的外围电路，忆阻器能够在存算一体范式下执行高能效计算，为边缘智能设备的实现提供了新的底层硬件解决方案。本次报告将介绍我们近年来在忆阻器器件、算法和芯片等方面开展的系统研究。研究结果展示了忆阻器在边缘智能系统构建中的潜力，同时也为开发基于自然界丰富的物理、化学特性的高能效智能硬件系统提供了参考。

D06-07

铪基铁电材料物性及器件可靠性研究

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铁电材料因其低功耗特性，长期以来被广泛应用于存储器中。近年来，铪基铁电材料由于在小于 10 nm 厚度下依然展现出铁电性，成为新一代器件尺度微缩的核心候选。该类铁电性被普遍认为源于极性正交相（$Pca2_1$），但 HfO_2在常温下稳定为非铁电的单斜相，在高温下则为四方相，这些结构均具有中心对称性，无法产生铁电性。实验与模拟研究发现，薄膜厚度、应力、掺杂、电场等是诱导铁电性的关键因素，第一性原理计算揭示了掺杂元素、界面能及其他协同作用对铁电相稳定性的重要影响。

本报告通过第一性原理计算仿真，深入探讨了纯 HfO_2与 Si 掺杂 HfO_2在有限尺寸与温度条件下的铁电相形成机制，重点研究了表面能、熵和极化反转能垒。在成核阶段，四方相（t 相）在掺杂和表面能共同作用下具有热力学优势；随着温度下降与晶粒生长，t 相会因低的转变能垒而转变为铁电正交相（o 相）。研究进一步识别出七种极化翻转路径，归类为两类，并指出两种类四方路径能垒较低，Zr 掺杂可进一步降低能垒，使其转变为对称性更高的 t 相，有望实现高效极化切换。此外，报告系统研究了 7nm HZO 电容器在高温下的可靠性问

题，首次在热循环中观察到“re-wakeup”现象。分析发现，晶界缺陷中的正电荷俘获会导致电畴钉扎，而高温下增强的电子注入效应可解除钉扎，重新激发极化行为。该现象揭示了热激发条件下缺陷演化与器件性能之间的深层关联，强调了晶界工程在提升超薄 HZO 可靠性方面的重要性。本研究结合热力学、动力学、器件结构与缺陷行为，全面揭示了铪基铁电材料的极化机制与可靠性调控规律，为优化铁电薄膜性能及其在未来高密度、低功耗存储器中的应用提供了理论依据与实践路径。

D06-08

二维半导体材料、器件与集成技术

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集成电路进入到“后摩尔时代”，需要寻求底层材料和电路架构的原始创新。二维半导体材料具有超薄极限的沟道厚度和低温后端异质集成等特点，是延续摩尔定律的终极路线，也是我国实现集成电路技术突围的路径之一。本报告将围绕硅基融合的集成芯片这一目标，介绍我们团队在二维半导体单晶外延制备、高性能晶体管器件、集成电路以及 AI 芯片方面的进展，梳理领域未来发展趋势和挑战，并介绍南京大学和苏州实验室在该方向的布局。

D06-09

氧化镓半导体功率电子器件

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超宽禁带氧化镓具有高临界击穿场强、高功率品质因子，可通过速度快、成本低的熔融法单晶生长获得，在能源、信息、国防领域具有应用优势。为充分挖掘氧化镓材料潜力，开展了（1）氧化镓 MOCVD 外延生长及表/界面微纳加工工艺研究：外延工艺、表面刻蚀、表面保护、界面退火和电偶极子层等工艺方案，解决了氧化镓界面缺陷高以及无终端结构器件性能差的问题；（2）高效终端方案设计与研制：开发了热氧高阻终端、结终端拓展、台面终端以及复合终端结构，开发了氧化镍载流子可控生长、选区热氧工艺、低损伤刻蚀工艺，有效抑制了边缘峰值电场，研制了大电流和高反向阻断能力的氧化镓功率二极管器件；（3）新晶体管结构设计与研制：采用热氧退火和 N 离子注入两种方案，首创氧化镓准反型沟槽晶体管（UMOSFET）。以上成果为氧化镓功率电子器件的电场和载流子调控提供了参考。

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D06-10

导体量子比特与微波谐振腔耦合研究

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近年来半导体量子计算取得系列进展，量子比特性能得到大幅提升，单比特和两比特量子门保真度均已达到容错量子计算阈值，如何进一步扩展比特数量成为该领域的重要议题。以微波谐振腔中的微波光子为媒介，不仅可以用来非破坏、高灵敏地探测比特，还能用于实现比特间的长程耦合，是半导体量子比特读出和扩展的一种重要方案。报告将介绍课题组近期实现的高阻抗微波谐振腔与半导体量子比特强耦合的工作，以及进一步利用谐振腔耦合与扩展半导体量子比特方面的相关进展。

D06-11

铁电氧化物薄膜晶体管三维集成

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基于铪基铁电与氧化物半导体的新型铁电薄膜晶体管铁电氧化物薄膜晶体管

由于其优异的存储器件特性与 CMOS 技术的兼容等特性成为未来高密度三维集成存储与存算一体系统的主要候选者，其三维单片集成技术成为人们广泛研究的重点课题。然而，传统的非晶氧化物半导体如 IGZO 等由于与铪基铁电薄膜材料在性质与制备工艺的不兼容性使得其实现三维单片集成面临巨大的挑战。

本报告将介绍一种与铪基铁电材料性质与制备工艺兼容的晶化 TiO2 半导体作为沟道的新型铁电薄膜晶体管器件及其三维集成的相关事宜，包括器件存储特性、可靠性以及实现三维高密度集成的潜力与所面临的挑战等。

D06-12

ALD 氧化物半导体器件缺陷表征与稳定性机理研究

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金属氧化物半导体材料因其宽禁带和低漏电的特性，是实现 DRAM 选通管半导体沟道的最佳候选材料之一。同时，将氧化物半导体器件与硅基 CMOS 集成电路技术相融合，实现逻辑与存储的单片三维集成，有望为集成电路性能提升提供新的技术途径。其中，厘清氧化物半导体器件可靠性机理与优化方法，实现高可靠性器件，是上述氧化物半导体器件技术面临的关键挑战之一。因此，如何表征和理解缺陷的种类和产生过程、如何澄清相关缺陷对器件性能及 DRAM 存储单元的影响十分重要。本次报告将介绍氧化物半导体器件可靠性与缺陷表征的研究进展，主要包括：1）ALD IGZO 器件中缺陷的光电表征、物理表征等表征方法与作用机理研究；2）ALD IGZO 器件的稳定性机理与优化方法研究。

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D06-13

半导体 Ge/SiGe 异质结栅控量子器件研究

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基于半导体栅控量子点的自旋量子比特方案具有与先进 CMOS 工艺兼容的优势，是可扩展化量子 计算最有潜力的候选方案之一[1, 2]。无掺杂 Ge/SiGe 平面异质结中的空穴载流子具有高迁移率、轻有 效质量、强自旋-轨道耦合的特点，是构筑电学栅控耦合多量子点器件的理想宿主材料[3]。采用兼容 标准半导体微纳加工的工艺，我们在该异质结上制备了多种低维栅控量子器件，在低温下系统研究了量子限域下的空穴量子输运特性。在载流子密度可调的场效应 Hall-bar 器件中提取和分析了与量子点构建相关的重要输运参数。以 整数量子霍尔效应及分数量子霍尔态迹象验证了无掺杂 Ge/SiGe 异质结该体系的低无序度，论证了量 子散射时间是衡量该材料量子输运质量和器件品质的关键指标[4]；以量子化电导台阶验证了无掺杂 Ge/SiGe 异质结的准一维量子限域特性，并展示了在量子限域条件下大 g 因子及其可调性；系统优化 了器件工艺和器件结构，构建了高质量的无掺杂 Ge/SiGe 异质结叠栅量子点器件，在 1.7 K 条件下实现 以库仑振荡与库仑菱形图样为标志的单空穴调控。

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D06-14

先进三维集成电路设计和工艺进展

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随着传统集成电路摩尔定律的逐渐失效，三维集成被认为是在芯片系统层面延续摩尔定律的必由之路。本报告将介绍三维集成的发展简史和最新的研究与应用进展。从狭义上来看，三维集成又可以分为准三维（或 2.5 维）和真正的三维集成两种方式。而真三维集成又可以分为单片三维（Monolithic）和基于封装的三维集成两种。本报告试图从工艺、设计和应用三个维度对这几种三维集成方式作分析和探讨，并介绍当前在这三个不同维度上的代表性研究单位（或者公司）及其研究成果（或产品）。

口头报告

D06-01

晶圆级相变存储材料纳米结构界面可靠性研究

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相变存储器（PCRAM）由于其优异的可微缩性，被认为是大容量非易失性存储器的未来选择。随着先进制程下节点的不断微缩，光刻工艺中控制关键线宽偏差和刻蚀工艺中减少相变材料边缘氧化，成为制备高密度高均匀性相变存储阵列的一大难点。同时小尺寸相变单元在经过重复相变操作的高电场和高热场作用后，电极材料和相变材料间容易发生原子扩散和组分偏析，因此理解高温相邻界面作用至关重要。

本研究使用亚分辨率辅助图形以优化工艺窗口，调控刻蚀参数以减少相变材料边缘氧化，制备了 sub-50 nm 小尺寸高均匀性的三明治结构相变存储阵列。通过原位加热实验结合能谱分析技术研究了三明治结构相变存储阵列高温下界面稳定性和元素偏析情况。实验设置四个温度，25℃，300℃，350℃，400℃。结果表明室温下相邻界面清晰分明，相变材料处于非晶状态，未受到光刻刻蚀工艺制备的高温影响；随着热处理温度的升高，富含 Ti 的下层 TiN 和 CGST 的界面逐渐出现了 Ti、Sb 和 Te 的互扩散并加重。过量的 Ti 促进了相变材料的解离，同时 Sb 和 Te 具有较高的扩散系数而向 TiN 移动，Ge 被排挤向上移动。因此靠近下层

的相变材料元素发生偏析而处于非晶状态，FFT 显示弥散衍射环。然而富含 N 的上层 TiN 和 CGST 界面一直保持稳定状态，靠近上层的相变材料处于晶体状态，FFT 显示 FCC 晶向。

本研究有助于了解电极材料和相变材料高温界面作用，理解相变单元经过重复操作后的失效机理以及给改善界面稳定性和提高相变存储器可靠性提供了思路，例如调控 TiN 原子比例或添加缓冲层。

D06-02

TaGeSbTe 相变存储芯片循环擦写失效机理研究

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随着人工智能和分布式传感技术在智能驾驶上的深度融合，车载电子系统对存储架构提出了极高的要求，尤其是在数据吞吐量和极端温度稳定性方面。相变存储器作为最成熟的非易失性存储器技术之一，在车载边缘计算节点中发挥重要作用。已有研究表明，Ta 掺杂 Ge2Sb2Te5（TaGeSbTe）材料具有低功耗、快速擦写和高热稳定性的特征，适合车载电子系统的适应场景。然而，操作过程中长期的电热应力引发相变材料的元素偏析与相分离，降低了器件的热稳定性和擦写寿命。因此，理解相变材料在循环擦写操作中的迁移行为及失效机理，对掌握这一技术至关重要。

本研究突破传统薄膜分析的局限，利用原位电子显微技术，引入低角度环形暗场像（LAADF）结晶动力学分析，揭示了芯片级循环擦写操作诱发的 TaGeSbTe 动态失效机制。结果表明，高温后道工艺（> 400 ℃）后，Ta 元素发生偏析，并聚集在相变材料外围。聚集区域的晶粒均为单一立方相（晶粒尺寸<10 nm），表明一定浓度的 Ta 元素降低了晶粒尺寸，与已有薄膜研究结果一致。然而，由于材料内部 Ta 原子的缺失，10^3 次循环擦写操作后即出现立方相与六方相共存。我们进一步观察到活性材料的元素迁移轨迹：通过高角度环形暗场像（HAADF）分析，未操作的初始态中 Ta 优先与 Te 成键，在原子级分辨率的能量色散 X 射线光谱（EDS）下显示出清晰的 $TaTe_2$ 纳米结构（Ta-Te 间距 0.285 nm）。经过 10^7 次循环擦写后，Ta 向底部 TiN 刀片电极迁移，Te 向顶部 TiN 电极迁移，$TaTe_2$ 数量减少至 28%，并伴随高阻态电阻下降约 50%。最终，循环擦写直至芯片失效，因 Ta 与底部 TiN 刀片电极中的 N 结合形成致密的 TaN 结构并包裹在底电极上方，导致 Reset-Stuck 失效。我们的研究还讨论了芯片的电学性能，包括不同循环擦写次数下的电阻漂移及开关特性。验证了 TaGeSbTe 芯片具有 125 ℃@1h 的数据保持力，小于百纳秒的操作速度，在进行 4×10^7 次循环擦写操作后仍保持超过 1 个数量级的电阻读取窗口，能够满足车规级存储芯片的要求。

D06-03

Microscopic Leakage Mechanism in Chalcogenide Ovonic Threshold Switching Selectors

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Ovonic threshold switching (OTS) selectors based on amorphous chalcogenide present a promising avenue for three-dimensional memory integration. As performance demands continue to escalate, leakage has emerged as a critical factor affecting the stability and reliability of selectors. In this study, we elucidate the leakage mechanisms in binary As_2Se_3-based OTS devices by revealing the local clusters in an amorphous structure. Utilizing four-dimensional scanning transmission electron microscopy (4D-STEM) combined with angstrom-beam electron diffraction (ABED), we directly observed titanium nitride (TiN) clusters enter the amorphous As_2Se_3 layer after first-fire, which is identified as the primary cause of leakage in such OTS devices. Based on this, incorporating a carbon buffer layer at the TiN/As_2Se_3 interface and annealing operation, the leakage current of the device can be effectively reduced and the durability of the device can be improved.

D06-04

低维材料及其电子器件的空间辐射效应研究

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随着商业航天与深空探测技术的迅猛发展，空间电子系统对高性能抗辐射器件的需求持续攀升，推动新型材料体系器件研发成为极端环境电子学的关键研究方向。石墨烯、碳管等低维材料通常因其本征高载流子迁移率、优异机械强度、高热导率等特性展现出巨大的潜力。然而，空间辐射环境中的高能粒子及高能光子等辐射因素可诱发晶格位移损伤与电离效应，在材料中引发晶格缺陷、陷阱电荷和载流子浓度变化等，从而显著劣化材料的电学、热学等性能。进一步地，在低维材料电子器件中中，辐射诱导的界面陷阱电荷和栅介质层电荷陷阱等会影响器件阈值电压和开关特性等，严重制约器件可靠性。因此，深入研究低维材料及其电子器件的辐射损伤机理及其与器件性能的关联规律，具有重要的价值。本报告将介绍我们在石墨烯、CNT、MoS_2 等低维材料及其电子器件的重离子及中子辐射效应损伤机理的研究进展，包括不同能量与注量的重离子/中子在低维材料中产生的缺陷性质的差异，以及器件电学和光学性能的变化规律。这些工作丰富了对低维材料与器件辐射效应的物理认识，建立了辐射损伤与电学性能的关联，为抗辐射低维电子器件的设计及其在空间中的应用提供了参考。

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D06-05

石墨烯在光电器件中的应用研究

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化学气相沉积（CVD）法制备的石墨烯具有光电性能优异、柔韧性好、稳定性高、隔离性好、可大面积制备的特点，在柔性光电器件领域具有广阔的应用前景。我们发展了 CVD 石墨烯的清洁无损转移、聚合物电解质掺杂调控石墨烯功函数和表面特性等方法，在柔性基体上获得了高透明导电性、表面平整且功函数可调的石墨烯薄膜。以其为透明电极开展了柔性光电器件的研制工作，获得了多种发光颜色的柔性有机发光二极管（OLED）器件（Proc. Natl. Acad. Sci. U. S. A. 2020, 117: 25991-25998; Nanoscale 2016, 8: 10714-10723; InfoMat. 2025, 7:e12638.）、国际上首个发光面积为 4 英寸的石墨烯基 OLED 器件（Nat. Commun. 2017, 8:14560）、透明 OLED 器件（Nat. Commun. 2022, 13:4987）、碳纳米管薄膜晶体管驱动的有源矩阵 OLED 显示器件（Small 2023, 2302920）、有机发光晶体管器件和高性能的石墨烯基柔性太阳能电池（Carbon 2021, 171: 350-358; Solar RRL. 2019, 3: 1900042; ACS Nano 2019, 13: 5513-5522; Nanoscale 2017, 9: 251-257）。同时，发展了离心涂覆制备转移介质以及直接利用转移介质作为一个支撑层的方法制备了石墨烯基柔性封装膜，可用于钙钛矿太阳能电池等光电器件的封装。

D06-06

Gaussian band trap in hetero-epitaxial β-Ga2O3 measured by photo-induced current transient spectroscopy

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β-Ga_2O_3 is a promising ultrawide bandgap material for power electronic devices and solar

blind UVC photodetectors. The high-resistivity Ga_2O_3 is widely used as a current-blocking layer in the power electronic or active layer of UVC photodetectors. However, the characterization of electronic defects in a highly resistive β- Ga_2O_3 is a tough challenge. Taking heteroepitaxy growth on sapphire as an example, the dominant growth challenge is the existence of six in-plane rotational domains due to the mismatch symmetric of the Ga_2O_3 epilayer and sapphire substrate, as well as the formation of structural defects like twin, stacking default, and so on. The resulting Ga_2O_3 epilayer surprisingly exhibits high resistivity, even for UID and doped Ga_2O_3, which does not happen in the Ga_2O_3 single crystals. It is suspected to be compensated by the structural defects. However, the energy levels and their roles are not revealed and understood yet. The technique of monitoring the transient of junction capacitance, namely, deep-level transient spectroscopy (DLTS), is a powerful tool to characterize trap levels. However, the DLTS is not applicable for high-resistivity semiconductors due to small junction capacitance and difficulties in injecting free carriers by a voltage pulse. Alternatively, photo-induced current transient spectroscopy (PICTS) can be used to characterize trap levels in highly resistive semiconductors.

Here we adapt temperature-dependent resistivity and photoinduced current transient spectroscopy (PICTS) for the first time to investigate the electronic defect of resistive β-Ga_2O_3 epilayer grown on a sapphire substrate. The temperature-dependent resistivity revealed a thermal activation energy of 0.27~0.48 eV. By PICTS, we observe a broad trap band instead of a discrete level, which can be expressed by a Gaussian peak centered at 0.3~0.4 eV with a standard deviation of 0.3 eV below the band edge. This trap band functions as a compensation defect, resulting in high resistivity, and also affects the falling time of the UVC photodetector. The broad trap can only be modulated a little bit by the degree of miscut angle of the substrate to a shallower energy level (<0.1 eV). It is suspected of originating from structural defects during growth. By constructing an ohmic metal semiconductor metal photoconductor, the highest responsivity and corresponding response time are 123.6 A/W and tr/tf of 1.24s/2.05s, respectively. This work highlights that we can accelerate the response time of UVC photoconductors by tailoring the structural defects in the future.

D06-07

Enhancement of Silicon Carbide Crystal Growth Rate by Pr, Ce, and La Solvent Additives in the Top-Seeded Solution Growth Method

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Using solvents to enhance the solubility of carbon in the silicon melt is an effective approach

to improve the efficiency of the top-seeded solution growth method for silicon carbide. This study proposes the use of rare earth elements (Pr, Ce, La) as solvent additives to enhance the growth efficiency of silicon carbide (SiC) crystals in the top-seeded solution growth (TSSG) method. A two-dimensional axisymmetric numerical simulation model was developed to analyze the thermal field, flow field, carbon solubility, carbon supersaturation distribution, and SiC growth rate in the Si-Ti-C, Si-Pr-C, Si-Ce-C, and Si-La-C melt systems. By optimizing key process parameters such as additive concentration, melt temperature distribution, crucible rotation speed, and seed crystal rotation speed, the maximum crystal growth rates in the Si-Ti-C, Si-Pr-C, Si-Ce-C, and Si-La-C systems were improved from 0.111 mm/h, 0.249 mm/h, 0.109 mm/h, and 0.093 mm/h to 0.643 mm/h, 5.171 mm/h, 3.285 mm/h, and 3.160 mm/h, respectively. Pr, Ce, and La additives enhanced the effective SiC crystal growth rates by approximately 8, 5.1, and 4.9 times compared to Ti as the solvent additive. Research reveals that using Pr, Ce, and La as solubility enhancers improves the efficiency of the top-seeded solution growth method for silicon carbide.

D06-08

液态金属基电磁功能材料

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液态金属基电磁功能材料以镓（Ga）及其合金为核心，兼具金属的高导电性、导热性和液体的流动性，具有低熔点、低毒性、自修复等独特优势。这类材料通过表面张力调控、尺寸变形和可烧结等特性，在柔性电子、传感器和电磁屏蔽领域展现出巨大潜力。在电磁屏蔽应用中，液态金属能有效填充材料空隙并构建导电网络，以介电损耗为主导实现高效屏蔽。通过动态填料设计，如超声共混制备的 Ga 基腻子可承受 1600%的应变并具备自修复能力，而磁性水凝胶通过添加 EGaInSn 和 Ni 填料可协同增强介电与磁损耗。此外，壳芯结构纤维织物和垂直相分离结构进一步实现了反射/吸收机制的可调控性，同时赋予材料疏水、耐水洗等实用功能。

液态金属还可通过原位反应构建多级电磁屏蔽体，Ga 氧化形成 In 核/氧化物壳结构，其缺陷和氧空位能显著增强极化损耗。通过还原沉积 Ag、Cu 等金属壳层（Ga-Ag 蛋黄壳结构），可实现多机制协同吸波，而双组份壳结构（Ga-CoNi）则能优化吸收带宽与反射损耗。作为填料，液态金属的高导电性和动态调控能力（磁性粒子掺杂）使其在柔性适配场景中表现优异；作为反应物，其多机制损耗和轻量化特性为高效电磁屏蔽提供了新思路。这些优势使液态金属基材料在可穿戴设备、智能响应系统等前沿领域具有广阔的应用前景，推动了柔性电磁功能材料的创新发展。

D06-09

纳米硅量子点的均匀制备与可控掺杂

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Silicon quantum dots (Si QDs) have attracted much attention nowadays because of their novel properties and potential applications in many kinds of nano-devices. In order to further improve the device performance, realizing effective doping in Si QDs is a crucial subject. However, the doping in nano-scaled semiconductors is quite complicated and difficult as revealed both in theoretical and experimental studies. Here, we report the systematically study on Phosphorus (P) or/and Boron (B) doping in Si QDs-based multilayers. The comparative study on the favourite occupy sites of P, B singly and co-doping in Si QDs has been carried out theoretically. We demonstrate the substitutional doping can be achieved even in the small-sized Si QDs experimentally and high conductivity can be obtained. It is also found that the light emission can be enhanced by suitable P doping. More interesting, the sub-band light emission has been observed for P-doped Si QDs and the corresponding model is proposed and the improved sub-band emission is realized by P/B co-doping.

D06-10

Regulation of energy band and luminescence properties in lead halide perovskite materials via lattice strain

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It is still quite challenging to achieve high-performance and stable blue perovskite materials due to their instability and degradation. The lattice strain provides an important pathway to investigate the degradation process. In this article, the lattice strain in perovskite nanocrystals was regulated by the ratio of Cs^+, EA^+, and Rb^+ cations with different sizes. Their electrical structure, formation energy and ion migration activation energy were calculated with the Density Functional Theory (DFT) method. The luminescence properties and stability of blue lead bromide perovskite nanocrystals were analyzed with spectra regulation from 516 nm to 472 nm. It was demonstrated that the lattice strain plays an important role in the luminescence performance and degradation process of perovskite materials.

Additionally, we observe the change in the lattice strain before and after the long-time stability test, indicating that the degradation of the local perovskite lattice structure could be the initial process for the long-term operation of perovskite materials. The luminescence properties,

stability and initial degradation of lead bromide perovskite nanocrystals have strong correlations with the lattice strain. This work provides useful guidelines in material design for both stable and high-performance blue perovskite materials as well as a new understanding of the initial degradation mechanism in perovskite materials with long-term stability.

D06-11

体相极化的优化与多场耦合调控的光电功能器件

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光电功能器件的性能高度依赖于其核心功能材料的物理特性，其中具有体相极化的铁电/压电材料在光生电荷分离、输运、能量转换等关键过程中扮演着决定性角色。然而，传统器件设计中体相极化的潜力常未被充分挖掘，且单一物理场（如电场、光场）的调控方式存在局限性。本研究聚焦无铅铋基铁电/压电材料，通过体相极化深度优化（调控组分、维度、微观结构与界面特性）与光、电、力、热等多物理场协同耦合调控，开发高性能多功能新型器件。采用先进材料设计（如梯度组分、A/B 位共掺、准同型相界、畴工程）实现了极化的精确调控。结合原位压电力显微镜、压电场多物理场模拟与第一性原理计算，阐明了电场-应力耦合下的畴翻转动力学与压电响应演化规律。研究表明，优化后的体相极化显著提升了光生载流子分离效率、输运能力并降低复合损失。引入多场耦合策略，系统揭示了多场（光、电、应力、温度）协同作用下体相极化的动态响应及其对器件光电性能（如转换效率、响应速度、探测率）的增强机制，实现了极化状态与器件响应的主动、动态、可编程操控，解锁了场致可调光电探测、力-光-电多模传感及高效能量收集等新颖功能。成功制备的原型器件（如太阳能光电催化器、光电探测器、铁电-光电生物传感器）实验证实了该策略在提升器件性能与拓展功能维度方面的显著优势。本研究的核心创新在于将体相极化优化与多场智能耦合调控深度融合，为突破现有光电器件性能瓶颈提供了新思路，不仅适用于铁电/压电/热释电等强极化材料体系，也为发展面向下一代智能光电子、柔性电子及集成光电子的高效多功能器件奠定了重要基础。相关工作以第一或通讯作者身份发表在 Nature Communications、Science Bulletin、Nano Energy、Advanced Functional Materials 等权威期刊。

D06-12

不同衬底对长波长 InGaN 基发光二极管中极化效应的影响

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硅衬底 GaN 基黄光 LED 的电光转换效率在 20 A/cm2 的电流条件下达到 24.3%，高于

蓝宝石和碳化硅。然而，高 In 组分的 InGaN/GaN 量子阱的发光效率受 InGaN 阱层压缩应变的影响较大，从而远低于蓝绿光的发光效率。本文通过构建 InxGa1-xN/GaN(x=0.3)超晶格模型研究蓝宝石、碳化硅和硅三种衬底上的 InGaN/GaN 量子阱异质界面处的载流子分布及输运情况，计算了三种衬底上的 InGaN/GaN 超晶格的电子结构与内部压电场，压电极化与片束缚电荷结合分析应变与晶体内压电场的响应机制。计算结果表明，与在蓝宝石和碳化硅衬底上生长的 InGaN/GaN 量子阱相比，硅衬底上的 Ga 面 GaN 的 InGaN/GaN 异质界面 VBO 明显减小，说明了空穴向 InGaN/GaN 量子阱有源区输运需要跨越的势垒高度降低，增加量子阱中空穴注入的可能性。电子性质结果表明极化效应产生的极化电场可以导致 InGaN/GaN 量子阱结构的带边三角形势阱改变成方形势。随着 InGaN 阱层压缩应变的释放，InGaN/GaN 量子阱的能带倾斜程度逐渐降低，一定程度上屏蔽了自发内建电场，有效弱化 QCSE。此外，压电极化效应分析表明，界面处的载流子分布及输运行为与极化反转有关。压电极化减小，压电诱导的片束缚电荷补偿了晶体内部的自由载流子，减少了有效活性区，增加了电子和空穴波函数在 InGaN/GaN 量子阱有源层重叠的几率。本文的理论结果揭示了硅衬底减小 InGaN 阱层压缩应变有利于促进空穴注入量子阱，并且增加电子—空穴对复合几率，提高内量子效率，进而提高 LED 光效的物理过程，揭示了双轴应变影响 InGaN/GaN 异质界面空穴输运及分布的物理机制，为设计量子阱结构继而提升 LED 性能提供理论指导。

D06-13

异质集成新型光电材料

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Hybrid bonding demonstrates significant application potential in the field of on-chip integrated opto-electronics. When combined with ion-slicing technique, this approach enables the fabrication of large-scale thin films of opto-electronic materials into SOI-like structures, thereby supporting the development of higher-performance novel devices. We have fabricated several heterogeneous substrates (including lithium niobate, lithium tantalate, silicon carbide, calcium fluoride, etc.) and demonstrated corresponding devices on-chip featuring rich functionality and outstanding performance, such as modulators, frequency combs and quantum networks.

D06-14

先进封装用苯并环丁烯基低介电常数材料的结构设计与性能优化

符文鑫

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随着 5G 通信与人工智能技术的发展，集成电路封装正经历从 2D 平面向 3D 异构集成的变革，对低介电常数（low-k）、高热稳定性封装材料提出迫切需求。本报告聚焦苯并环丁烯（BCB）基聚合物材料，围绕分子设计、界面调控及产业化应用，汇报近年来在先进封装材料领域的研究进展与性能突破。在分子设计层面，通过引入氟化策略与大位阻基团（如四苯乙烯），开发了本征低介电 BCB 单体（介电常数低至 2.5，10 GHz）。在有机 - 无机复合体系中，采用“化学键合-拓扑调控-分子组装”策略，通过硅烷偶联剂实现中空二氧化硅纳米粒子与 BCB 基体的共价键合，构建双稳定界面结构，使复合材料介电常数降至 2.12，介电损耗维持在 10^{-4}量级，同时热稳定性（Td5%＞445℃）与力学性能（模量 4.1 GPa）显著提升。针对产业化瓶颈，开发了“聚合-后修饰”模块化合成技术，实现 BCB 功能化聚硅氧烷的高效制备，并建成十公斤级中试生产线。相关材料已在扇出型晶圆级封装（FOWLP）、微波集成电路（MMIC）中完成工艺验证。本研究为解决我国高端封装材料“卡脖子”问题提供了新路径，未来将进一步探索 BCB 材料在 6G 太赫兹器件与柔性电子中的应用潜力，推动“低介电-高可靠-可定制”封装材料的自主化进程。

D06-15

顺次集成异构 CFET 材料转移关键工艺研究

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近年来，人工智能和高性能计算的快速发展对集成电路基础器的性能与集成密度提出更高要求。由于受到极端尺度下短沟道效应与制造工艺技术条件限制，进一步实现 MOSFET 尺寸微缩和电路综合性能大幅提高面临巨大挑战。顺序集成的垂直互补晶体管（CFET）架构可在一定程度上突破传统“摩尔定律”的尺寸微缩限制，大幅提升器件与电路的集成密度，成为了集成电路器件结构创新的重要发展方向，

设计一种底层为 P 型外延 Si FinFET，顶层为 N 型 NS GAAFET 的顺次集成异构 CFET 架构，可以使 NMOS 与 PMOS 载流子迁移率均达到较高水平，进而提升器件及电路综合性能。针对该种顺次集成异构 CFET 集成工艺中腐蚀 Si 对 GeSi 材料高选择比停止的技术难题，开发了 Si0.7Ge0.3/Si 叠层材料选择性腐蚀关键技术，探索出通过低温 TMAH 溶液实现刻蚀 Si 对 Si0.7Ge0.3 高选择比停止方案，选择比达到 109：1，为顺序集成异构 CFET 器件的制备提供了关键技术基础。

D06-16

高 chi 值嵌段共聚物 DSA 研究

石玲英

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导向自组装（DSA）是纳米光刻技术的重要备选方案之一，这种方法是嵌段共聚物自组装与传统光刻技术的完美结合，可以突破传统“光学+掩膜”的技术原理，有望突破光学极限，将纳米光刻推向更小的尺寸节点。目前国际上 DSA 研究主要应用的嵌段共聚物材料是 PS-b-PMMA，然而其周期尺寸通常大于 24nm。因此，DSA 向小尺寸节点的发展，需要发展新的嵌段共聚物自组装材料以及图案化工艺。我们在近五年的研究中，设计合成了一系列高相互作用参数低聚合度（高 chi 低 N 值）嵌段共聚物材料，系统研究了自组装行为，构建了一系列周期尺寸为 10-22 nm 的自组装结构库。进而展开了薄膜自组装取向性与长程有序性物理方法的研究，通过一步刻蚀法，制备了高稳定性以及高界面清晰度点、线、面纳米图案，进而在导向模版中实现了稳定的密度倍增导向自组装。该研究为小尺寸 DSA 纳米光刻技术提供了新材料以及相应的自组装技术，为 DSA 技术向小尺寸节点发展提供了科学依据。

D06-17

Study of high aspect ratio Polycrystalline silicon dry etching with size-selectivity for 3D DRAM parasite channel IGZO cutoff

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In multilayer stacked 3D devices, it is essential to completely expose the dummy protection layer in to finish IGZO cut and remove the parasite channel. We propose a high aspect ratio (HAR) Polycrystalline silicon trench etching method to expose the sidewall dummy protection layer. Due to the complexity of the 3D structure, it is very necessary to avoid damaging the IGZO behind the protection layer, so multiple ways of HAR trench Polycrystalline silicon etch are attempted. In this study, we investigate three ways of HAR Polycrystalline silicon trench etch, using wet, Bosch process, and two step size selective dry etching respectively. The wet process will damage the dummy protection material on the IGZO side wall due to the material native oxidation and loading effect of CMP process, which will damage IGZO in the subsequent process. The Bosch process has poor selectivity ratio between poly and HM, resulting in severe hard mask (HM) loss. Therefore, we adopt a two-step dry etching scheme with size-selective etching. Firstly, anisotropic etching is applied to make the “V” shape etch profile, then isotropic etch was used to fully remove the remaining Polycrystalline silicon in the trench. The two steps can be performed in the same chamber subsequently. The experimental results show that the size-selective two-step dry etching scheme can fully remove the trench Polycrystalline silicon and exposes the mentioned dummy protective layer without etching the native oxide layer and touch IGZO material. The results of this study can significantly reduce the risk of IGZO damage in 3D device fabrication by completing the IGZO parasite channel cutoff and avoiding channel-to-gate damages.

D06-18

基于自对准高 k 金属栅垂直沟道晶体管的源漏注入掺杂仿真与制备研究

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由于垂直沟道晶体管固有的三维结构限制，产生了诸如假栅形成困难和阴影效应等问题，为源漏注入掺杂带来了巨大的挑战。基于上述问题，本研究提出了一种无需假栅的离子注入方法，充分利用垂直沟道晶体管的几何特性形成的自遮蔽效应，成功实现了源漏注入掺杂的同时避免杂质进入沟道。同时采用 TCAD 仿真，系统研究了不同注入条件对垂直沟道晶体管性能的影响，揭示了在垂直沟道晶体管源漏区域天然形成的轻掺杂区所发挥的重要作用。最终，采用该离子注入方法成功制备了 N 型与 P 型垂直沟道晶体管。

D06-19

Morphological and Strain Engineering of SiGe Cladded Channels for Stacked Nanowire Transistors

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This paper presents a comprehensive study of silicon germanium (SiGe) cladded channels for stacked nanowires (NWs), focusing on morphological control and strain engineering to enhance device performance. High-resolution transmission electron microscopy (HRTEM) was used to characterize the Si NWs and SiGe cladding morphology. The results demonstrate that the morphology of SiGe cladding can be controlled by adjusting the high-temperature H2 baking conditions, leading to shapes such as triangular, circular, and hexagonal. TCAD simulations and geometric phase analysis (GPA) of TEM images revealed that the maximum compressive stress of SiGe cladding is 3 GPa, corresponding to a compressive strain of 2.48%, which significantly enhances hole mobility. Electrical performance tests and simulations on PMOS devices with different morphologies showed excellent short-channel effects (SCEs) control, with a subthreshold swing (SS) of approximately 70 mV/dec and a drain-induced barrier lowering (DIBL) of only 40 mV/V. These findings provide valuable guidelines for fabricating high-quality SiGe channels with controlled structures, enabling the realization of high carrier mobilities in future devices.

D06-20

Fabrication and Characterization of Mo/MoC Thin Films for Interconnect Applications in Ultra-Large-Scale Integrated Circuits

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With the continuous scaling of integrated circuit technology to the 7-nanometer node and beyond, traditional copper interconnect technology faces significant challenges due to rising resistivity and declining reliability. This study explores molybdenum/molybdenum carbide (Mo/MoC) thin films as a promising alternative for interconnect materials in ultra-large-scale integrated circuits. The Mo/MoC thin film structures were fabricated using reactive magnetron sputtering, followed by systematic characterization of their electrical, thermal, and interfacial properties. Electrical performance testing based on the Vanderbilt method revealed that the resistivity of Mo/MoC thin films is approximately 5.09/5.53 μΩ·cm, demonstrating conductive performance comparable to copper interconnects. Annealing experiments at 450/550 ℃ confirmed their excellent thermal stability, with no significant interfacial diffusion observed. This study demonstrates that Mo/MoC thin films, as a new generation of interconnect materials, can effectively address the technical bottlenecks of copper interconnects in advanced manufacturing processes, offering significant potential for practical applications.

D06-21

先进电子封装用多功能环氧树脂研究进展

罗裕波

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6G 通讯、人工智能、工业 4.0 等国家重大战略需求对电子器件的功率和集成度提出了更高的要求，热流密度越来越高，若无法有效排散，将导致结温急剧上升，键合线剥离、芯片裂纹等热失效概率急剧增加，使用寿命显著降低。与此同时，数据安全和信号保真对芯片等电子元器件的抗电磁干扰能力也提出了更高要求。传统封装环氧树脂热导率低、透波、热膨胀系数大、易燃等限制了其在先进电子封装中的应用。先进电子封装要求其封装环氧树脂高热导率以促进结温快速散失、吸波以减少电磁波的干扰，保护设备的正常运行、低热膨胀系数以降低热膨胀系数不匹配引起的热失效，阻燃以降低热失控引起火灾的概率。本文从材料成分及结构设计、仿真模拟及实验验证等系统性地研究了先进电子封装用导热、吸波、阻燃、低膨胀等多功能环氧树脂设计制备及性能调控，为先进电子封装提供新材料及方法。

D06-22

Cu 基板上 Bi 镀膜工艺的优化及润湿性评价

孟日欣

燕山大学

高温无铅焊料用 Bi 基合金因熔点适宜、环境友好、价格低廉而备受关注。但 Bi 基焊料

与 Cu 基板之间的润湿性差，影响其焊点的可靠性。本研究采用在 Cu 基板上电镀 Bi 拟改善其润湿性。在前期电镀 Bi 工艺的基础上，本研究从预处理过程以及镀膜过程两部分对该工艺进行了进一步优化，并将 Bi-2.5Ag、Bi-5.0Ag 以及 Bi-2Ag-0.5Cu 焊料与镀 Bi 的 Cu 基板焊接后，采用铺展面积法和润湿角法对焊料润湿性能进行了表征。结果表明，在预处理部分，选用电解抛光代替手工打磨处理 Cu 基板，并添加 H2O2 活化 Cu 基板，镀层中 Bi 晶粒尺寸更均匀细小，平均晶粒约为 300 nm，润湿性也显著提升。镀膜过程中，润湿性随镀液流动性的上升先改善后减弱，转子转速为 80r/min 时润湿性最佳；转子转速为 80r/min，160r/min 时镀层呈现网絮状组织；当转子转速为 240r/min 时网絮状组织消失。

墙报

D06-P01

Bi-Se ovonic threshold switch selector and threshold voltage drift

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Selector devices play a critical role in large-scale storage arrays. Ovonic threshold switching (OTS) devices are recognized as highly suitable memory elements due to their capacity to suppress leakage currents while ensuring efficient and reliable operation. Nonetheless, threshold voltage drift presents a significant challenge that can potentially compromise the reliability of data read/write operations. Consequently, investigating OTS switches with low drift coefficients is of considerable importance. In this study, a bismuth-selenium (Bi-Se) OTS device was fabricated using magnetron sputtering. Testing demonstrated that when the bismuth-to-selenium ratio is 1:4, the device exhibits an exceptionally low drift coefficient.The drift coefficients of devices composed of Bi_1Se_9 and Bi_1Se_4 are measured at 30 mV/dec and 0 mV/dec, respectively. To elucidate the underlying mechanisms that contribute to this low drift, we employed a combination of physical characterization techniques alongside first-principles calculations for preliminary analysis, and the threshold voltage is influenced by defect states, and the drift of the threshold voltage may be associated with relaxation processes in the microstructure.

D06-P02

基于铟镓锌氧（IGZO）薄膜材料的薄膜晶体管研究

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本研究采用铟镓锌氧（IGZO）薄膜作为核心功能材料，其宽禁带特性赋予亚皮安级关

态电流，同时 IGZO 材料具有低温大面积沉积的特性，使其成为三维集成上层器件的候选人。那么，有效改善 IGZO 器件的性能具有一定的必要性。本文研究了无退火以及沟道预退火后的器件性能差异，不同等离子处理方法对器件性能的影响影响。结论表明，具有沟道预退火的器件相较于无退火的 IGZO 器件驱动提升 3.8 倍；通过涂胶-刻蚀-干法去胶等离子处理之后，器件的驱动提升了 20%。IGZO 新材料通过沟道预退火以及涂胶-刻蚀-干法去胶等离子处理之后，IGZO 器件的驱动具有大幅提升，使得其与 Si 基器件更加的匹配，使其超低关态电流突破“功耗-密度”权衡瓶颈，结合低温工艺兼容性为 CMOS 后端集成提供新范式，并为 AI 边缘计算构建速度-密度-能效协同优化平台。

D06-P03

Channel current noise analysis of silicon-based nano-MOSFETs

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In silicon-based nanoscale metal-oxide-semiconductor field-effect transistors (MOSFETs), with the enhancement of short-channel and quantum effects, the characteristics of channel current noise undergo notable changes. Two main aspects are observed: first, gate carrier tunneling through the thin oxide barrier generates gate tunneling shot noise, which is suppressed by Coulomb interaction and Fermi statistics; second, the cross-correlation noise between the induced gate current and the drain current increases. Addressing this phenomenon, based on the structural characteristics of silicon-based nano-MOSFETs, this study constructs a complete model containing four key noise components: suppressed drain-source shot noise, suppressed gate tunneling shot noise, short-channel-effect-modified thermal noise and cross-correlation noise. Then, Monte Carlo simulation is further used to determine the channel current noise composition of silicon-based nanoscale MOSFETs, and the evolution of the noise characteristics is systematically investigated under different bias voltages, operating temperatures, and substrate doping concentrations. The theoretical results are basically consistent with the simulated results, and the channel noise increases with the increase of bias voltage. This achievement holds promise for enhancing the operational efficiency, reliability, and lifetime of nanoscale small-sized MOSFET devices.

D06-P04

侧墙 SiNx 材料选择性刻蚀的关键工艺

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本文中针对侧墙 SiNx 材料选择性刻蚀的关键工艺展开研究，通过分析磷酸溶液中 SiNx 刻蚀的反应机理，提出了刻蚀溶剂设计、反应条件调控和薄膜工艺的协同优化，实现 SiNx/SiO_2/HfO_2 叠层结构的高选择性刻蚀。针对常规的磷酸溶液中 SiN_x/SiO_2 的刻蚀选择比及 HfO_2 层易被刻蚀的问题，提出了将有机溶剂加入 85wt. % 磷酸溶液形成混合刻蚀溶剂的方案。在反应环境为 160 ℃下实现了 SiN_x/SiO_2 的刻蚀选择比高于 104:1，同时将 HfO_2 刻蚀速率进一步降至 0.2 Å/min 以下，从而 SiN_x/HfO_2 的刻蚀选择比提高至 900:1，同步实现了 SiN_x/SiO_2 和 SiN_x/HfO_2 超高刻蚀选择性。同时，研究了 SiN_x/SiO_2/HfO_2 叠层结构在小尺寸的窄缝结构中 SiN_x 材料刻蚀速率对反应环境中温度敏感性和时间依赖性的影响。当刻蚀温度从 120 ℃增加至 160 ℃的过程中，PE SiN_x 的刻蚀速率显著增加至 11.47 nm/min，而随着刻蚀时间的增加，受限于窄缝结构的影响，SiN_x 的刻蚀速率逐步下降。通过溶剂-材料-工艺的协同工艺系统性研究了 SiN_x 材料湿法刻蚀中出现的选择比不足，小尺寸叠层刻蚀过程中刻蚀速率等难题，为实现全空气侧墙结构 GAA NSFET 器件提供了指导。这为 3 纳米以下节点 CMOS 逻辑器件的创新结构具有重要应用价值。

D06-P05

TiN、TaN 和 TiAl 金属功函数膜层对阈值影响及单元电路验证

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在 GAA CMOS 器件中，阈值电压的对称性对于器件和电路性能的优化至关重要。较低的阈值电压会产生较大的漏电流，而漏电流是衡量静态功耗的一个重要标准。正常工作的 CMOS 电路需要较为对称的阈值电压，N/PFET 之间的阈值偏移应小于 100 mV，以减少因阈值电压失配导致的电路不稳定等问题。合理的阈值调控不仅能提高电路的整体稳定性，增加电路可靠性，还能在保证电路性能的同时降低漏电流和动态功耗。主要研究了通过原子层沉积（ALD）制备的栅电极厚度对器件阈值电压（Vt）的影响。我们设计了 TiN、TaN 和 TiAl 三种常见高 κ 材料的厚度变化实验方案，以探索实现对称阈值的有效方法。通过系统分析不同 HK 层厚度对 GAA CMOS 器件电学特性的影响，我们最终获得了对称阈值（±0.35V）CMOS 器件，并为这一目标提供了实验依据。

D06-P06

Optimal Stoichiometry and Performance Evolution in As-Se Based OTS Devices

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Arsenic-selenium (As-Se) based ovonic threshold switching (OTS) devices are pivotal building blocks for enabling practical non-volatile memory technologies. In this work, we

investigate the performance evolution of As-Se OTS devices with varying As contents. A non-monotonic trend is observed in device performance: the leakage current first decreases and then increases with increasing As content, while the threshold voltage exhibits an opposite trend. The device with 50% As demonstrates minimized leakage and superior endurance characteristics. Molecular dynamics simulations reveal that at low As content, Se-Se homopolar bonds are prevalent, but these bonds are significantly suppressed at the intermediate composition. At higher As concentrations, As-Se heteropolar bonds decrease, while As-As bonds become dominant. Coordination number analysis shows that the average coordination number at 50% As closely approaches the ideal threshold of 2.4, indicating optimized network rigidity. Additionally, electronic structure analysis shows that the bandgap is maximized at the 50% composition, corresponding to significant contributions from both As and Se p-orbitals. These findings identify the optimal As-Se stoichiometry for high-performance OTS devices and provide valuable insights for material and device design.

D06-P07

非晶氧化物薄膜晶体管的低温电学与低频噪声特性研究

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非晶氧化物薄膜晶体管（AOS TFTs）已被广泛应用于大面积传感领域。尤其在粒子对撞机、天文观测和地球遥感等特殊应用中，图像传感器需在极低温环境下工作，因此必须研究 AOS TFTs 的低温性能。本研究针对两类具有不同源漏电极的 a-IZO TFTs，测量并分析其在 10K 至 300K 的低温电学特性与低频噪声特性。对于具有金属电极器件，随着温度升高，a-IZO 沟道在 80K 时发生载流子输运机制转变，从变程跳跃导电转变为能带导电。噪声测试表明，该器件在低温下由界面陷阱主导型转变为体陷阱主导型；对于具有半导体电极器件，源漏接触噪声在低温区域出现并成为主要噪声源，当温度升至 120K 以上时，沟道噪声转为主导噪声源。接触噪声对总低频噪声的贡献度取决于沟道电阻与接触电阻的比值。

D06-P08

Impact of Low-k Inner Spacers on GAAFET Capacitance and Channel Stress at Advanced Nodes

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As Gate All Around Field Effect Transistors (GAAFETs) scale toward advanced nodes, the Inner Spacer plays a dual critical role. Its evolution toward lower dielectric constants (k values)

reduces parasitic capacitance and improves RC delay, yet its material properties simultaneously govern mechanical stress transfer from source/drain regions to the channel, directly influencing carrier mobility. This work employs comprehensive technology computer aided design (TCAD) simulations to investigate the trade-off between capacitive parasitics and stress engineered performance in scaled GAAFETs. We analyze the impact of Inner Spacer k values and intrinsic material properties, such as Young modulus, on total gate capacitance and longitudinal channel stress profiles. Results demonstrate that while ultralow k Inner Spacer materials minimize capacitance, they significantly degrade beneficial uniaxial compressive stress in PFET channels and tensile stress in NFET channels, incurring performance penalties. This study quantifies these critical dependencies and provides guidelines for optimizing Inner Spacer material selection to maximize device performance at sub 3 nm nodes.

D06-P09

Study of Loading Effect of Cavity etching for Inner Spacer Module Process

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In Gate-All-Around (GAA) process, the inner spacer is used to isolate the gate and the source/drain to reduce parasitic capacitance. However, there are few reports on the development details of this process. The module involves multiple new steps, among which cavity etching is particularly critical and challenging. The depth of cavity etching determines the size of the inner spacer and indirectly defines the effective gate length. It also affects the value of parasitic capacitance and parasitic resistance. Meanwhile, in order to meet the demands of process, the cavity etching requires extremely high precision control and high selectivity to Si. In this paper, we study the cavity etching in dense arrays with small pitch (<100 nm) through experiments and simulations. The simulation results show that there is loading effect on dense structures in cavity etching at small size. This phenomenon is also verified in the experiment. In addition, we also study the root cause of the loading effect and how to alleviate this effect in cavity etching of dense array. We propose a multi-step etching method and it successfully reduce the loading effect. The dense array structure studied in this paper is closer to the actual situation and is expected to provide a reference for the industrial manufacturing of GAA devices.

仅发表论文

D06-PO01

Interfacial Investigation of Photosensitive Polyimide and Metallic Copper under In Situ Transmission Electron Microscopy

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The interfacial stability between polymer-based macromolecular materials and metallic components in advanced packaging architectures plays a critical role in enhancing chip reliability. Current research on photosensitive polyimide/copper (PSPI/Cu) interfacial properties suffers from insufficient empirical data due to significant material property disparities, nanoscale interfacial dimensions, and methodological limitations, particularly regarding interfacial failure mechanisms induced by ionic migration. Therefore, the research on the performance of the PSPI/Cu interface is of great significance. Utilizing in-situ heating transmission electron microscopy (TEM), we dynamically monitored the nucleation and migration behavior of nanoparticles at the PSPI/Cu interface with atomic-scale resolution. Experimental observations revealed the nanoparticle evolution process: initial nucleation distant from the interface, subsequent thermal growth, and final stabilization as discrete spherical particles (average diameter approximately 10 nm). Mechanistic analysis indicates that nanoparticle formation originates from two synergistic factors: (1) chemical interaction between hydroxyl ions (OH^-) from the polyimide precursor solution and copper substrate during imidization, and (2) oxygen permeation through the PSPI matrix, which facilitates copper oxidation and subsequent nanoparticle coarsening. These phenomena ultimately lead to interfacial void formation and mechanical decohesion. The findings establish a theoretical framework for optimizing photosensitive polyimide formulations and process parameters, offering critical guidance for enhancing thermal stability in the redistribution layer (RDL) technologies for next-generation advanced packaging applications.

D06-PO02

Research on the Mechanical Properties of Thermal Interface Materials at the Microscale

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In advanced packaging, thermal interface materials (TIMs) effectively fill irregular gaps between chips and heat sinks caused by surface roughness, establishing continuous thermal conduction networks at solid-solid contact interfaces to enhance the heat dissipation efficiency of packaging systems. As a critical material in advanced packaging systems, the synergistic

optimization of their mechanical properties and thermal conductive characteristics is pivotal for improving device reliability. Current studies predominantly evaluate material performance through macroscopic mechanical parameters, while systematic investigations on the fundamental microscopic fracture mechanisms governing mechanical behavior and their intrinsic correlations with macroscopic properties remain insufficient. To address this, this study fabricated alumina (Al_2O_3)-filled TIMs with filler loadings of 70 wt%, 80 wt%, and 90 wt%, respectively. In-situ scanning electron microscopy (SEM) was employed to monitor real-time microstructural evolution under mechanical loading while synchronously acquiring micron-scale mechanical response curves. The influence mechanism of filler content on the micromechanical behavior of composites was systematically investigated, with particular emphasis on structure-property relationships between microstructural characteristics and macroscopic mechanical performance. Experimental results demonstrated that as Al_2O_3 content increased from 70% to 90%, the fracture elongation exhibited a nonlinear decreasing trend, with the 80 wt% composite showing optimal comprehensive mechanical properties (392% elongation at break, 0.93 MPa tensile strength, and 1.50 MPa elastic modulus). Microstructural analysis revealed that the medium-filled system (80 wt%) developed uniform and dense microcrack networks during stretching, whereas low/high-filled systems (70 wt%, 90 wt%) generated stress-concentrated crazing that initiated crack propagation. This study elucidates the structure-property relationship between microscopic fracture mechanisms and macroscopic mechanical responses in highly filled polymer composites, providing theoretical guidance for developing high-reliability TIMs.

D06-PO03

Enhancing Transmission and coupling Efficiency in Cassegrain Optical Systems with Four-Petal Gaussian Beams

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This study investigates the propagation characteristics of four-petal Gaussian beams through Cassegrain optical system. With the properties of this new type of beam, the problem of masking loss in the Cassegrain optical system can be well solved. Analytical expressions of the optical field for beams after propagating the optical system are derived, considering atmospheric turbulence effects and random jitter on coupling efficiency. Simulation tests explore various factors affecting transmission efficiency. Acceptable axial mounting error tolerance and significant efficiency drops beyond specific communication distances under different turbulence conditions (C_n^2). Achieving over 80% coupling efficiency is feasible with specific lens parameters

(f=0.4-0.5 mm, receiving position after 4 km) using standardized lenses. This work offers a theoretical model for four-petal Gaussian beams, aiding optical communication design and application, with practical engineering implications.

D06-PO04

Study on Interfacial Mechanical Properties between Advanced Packaging Material Photosensitive Polyimide and Copper Metal

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In the field of integrated circuits, as the physical limits of Moore's Law approach, advanced packaging technologies are increasingly becoming a key and effective driving force for enhancing integrated circuit performance in the post-Moore era. However, the interfacial stability of advanced packaging materials, represented by photosensitive polyimide (PSPI), directly determines the reliability of chips and devices within integrated circuits. Since the thickness of PSPI films prepared by spin-coating processes is typically controlled on the order of 10 μm or even lower, research on the interfacial stress distribution and molecular-level interfacial bonding mechanisms at the heterointerface formed between PSPI and copper metal at the sub-micron scale faces significant challenges compared to the characterization of traditional macroscopic material properties. Based on this, a study was conducted on the mechanical response mechanism of the photosensitive polyimide/copper metal heterointerface under external loading. An in situ experimental platform was employed to observe the interfacial fracture failure process in real-time, revealing the dynamic evolution of interfacial delamination failure under load. The high-resolution imaging mode of Atomic Force Microscopy (AFM) was utilized to characterize the surface morphology and interfacial diffusion layer features within the interfacial region. Simultaneously, nanoindentation technology was combined to obtain the gradient distribution of the elastic modulus in the interfacial transition zone between photosensitive polyimide and copper metal. Through in situ testing, AFM characterization, and nanoindentation techniques, the mechanical response mechanism at the PSPI/copper metal interface was characterized, and its interfacial failure mechanism was revealed. By comparing sample data under different processing conditions, this work provides a scientific and effective theoretical basis for the optimization of advanced packaging materials and process improvements.