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D06. 先进微电子与光电子材料

分会主席：赵超、俞文杰、杨德仁

D06-I01

最终交流类型：邀请报告

半导体相变存储器

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智慧城市、5G、物联网、云计算、人工智能等 “大数据”的兴起对计算机架构提出了更高的要求，从冯诺依曼架构发展到存算一体架构是必然趋势。相变存储器（PCRAM）具有非易失、微缩性能好、与 CMOS 工艺兼容、循环寿命长、高速读取、可三维集成等优点，被认为是最具潜力的下一代非挥发存储技术。PCRAM 可以填补 DRAM 与 FLASH 之间的性能鸿沟，解决目前计算机机架构中“存储墙”的问题，也可以作为神经形态芯片实现类脑计算，将会在数据中心、汽车电子、物联网和人工智能等方面获得大规模应用。报告介绍了课题组近年来在相变存储器研究方面的进展，包括相变材料可逆相变机理、高速相变材料、高性能开关材料与机理，相变存储器产业化进展等。

D06-I02

最终交流类型：邀请报告

硅基硅锗材料的分子束外延生长

张结印 [1,2]，明铭 [1,2]，王建桓 [1]，刘方泽 [1]，张建军 [1]

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硅锗不仅是集成电路先进节点的沟道材料，也是半导体量子计算的核心材料。分子束外延制备硅锗材料的优点主要体现在两个方面，一方面可以获得原子尺度尖锐界面的异质结；另一方面它可以在 400°C 以下的低温制备高质量的硅和硅锗单晶薄膜，即可以在硅基器件上进行二次甚至多次硅（锗）或硅锗材料外延，实现特定硅基材料和器件的异质异构集成。本报告主要介绍我们研究组小组最近几年通过分子束外延生长制备一维量子线和二维异质结薄膜方面的研究工作，包括可控制备高质量的一维锗和锗硅量子线材料，以及 SiGe/Si/SiGe、SiGe/Ge/SiGe 高质量二维异质结电子气、空穴气材料等。

D06-I03

最终交流类型：邀请报告

先进围栅器件关键工艺与新结构器件研究

张青竹 [1]，蒋任婕 [1]，曹磊 [1]，姚佳欣 [1]，张学祥 [1]，桑冠荞 [1]，王鹏 [1]，李恋恋 [1]，张渼荷 [1]，张亚东 [1]，张兆浩 [1]，李庆坤 [1]，殷华湘 [1,2]

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2. 中国科学院大学 集成电路学院

随着互补金属氧化物半导体（CMOS）集成电路特征尺寸（CD）不断缩小，主流鳍式场效应晶体管（FinFET）面临着迁移率退化、栅控能力减弱、漏电流和功耗增加的难题，采用围栅（GAA）器件结构是未来集成电路发展的趋势。兼容主流 FinFET 工艺的堆叠硅纳米片（SiNS） GAA 器件具有栅控和驱动性能明显优势，已经成为 Samsung、TSMC 和 Intel 等所有国际巨头 3-2 nm 技术代器件结构。针对新围栅器

件制备面临的关键工艺挑战，先后完成 GAA 堆叠 SiNS 器件工作机理探索、流程设计、关键工艺研发、阈值调控和 CMOS 器件/电路研制工艺的理论和技术体系的先导研究。此外，针对 GAA NS PFET 载流子迁移率低难题，设计新型鱼骨形（Fishbone） FETs，提升器件驱动性能，采用单一金属功函数层，实现对称阈值电压，且 N/P 型器件的驱动性能相当，克服了 GAA PFET 载流子迁移率低难题，并首次在体硅衬底上研制 CMOS 型 FishboneFET 和 TreeFET 器件。

本报告主要 GAA 堆叠 SiNS MOSFET 制备的关键工艺、模块技术和器件集成技术方面研究进展，重点讲述纳米片释放、沟道表面处理、漏电控制和阈值调控方面取得核心技术突破，并探索可增强栅控特性的新结构器件，包括 Fishbore FET、混混合晶向沟道 CFET、混合沟道 SRAM 等方面内容。

D06-I04

最终交流类型：邀请报告

硅基半导体量子点量子比特研究

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半导体量子点是实现量子计算的有力候选者之一，近几年课题组在硅基金属氧化物半导体（Si-MOS）和棚顶型锗纳米线材料体系上进行了一系列实验探索。在 Si-MOS 量子点中，实现了电子自旋弛豫时间关于外磁场大小和方向各向异性的高效调控，弛豫时间被提升两个量级；利用泡利自旋阻塞原理实现了自旋量子比特的操作和读取，并证明了噪声鲁棒的读取方案；通过模拟微磁体参数寻找到量子比特操控的最优工作点，并基于翻转模式的电偶极自旋共振将比特操控速度提升一个量级；进一步证明了保真度超过 99 % 的单比特门操作，达到容错量子计算的阈值条件，同时基于几何量子计算实现了噪声鲁棒的量子比特门操作；发展了校正波形畸变的方案并在此基础上实现两比特 SWAP 门操作。在锗纳米线空穴量子点中，利用空穴自旋具有强的自旋轨道耦合效应，实现了空穴自旋 g 因子的各项异性测量和自旋轨道耦合强度高效调控，利用电偶极自旋共振实现了国际上最快的自旋量子比特操作，速度达到 540 MHz，并进一步将其提升至 1.2 GHz，同时研究了操控速率随着电场变化的高效调控。上述研究成果，为进一步实现高保真度的多量子比特操控奠定了坚实基础。

D06-I05

最终交流类型：邀请报告

硅基原子掺杂体系的自旋量子比特调控

贺煜 [1]

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硅基量子计算是目前比较有潜力的一类量子计算体系。其中，在基于掺杂原子的硅基量子计算方面，之前 20 年取得了长足进步。下一阶段的核心研究是研发面向大规模可扩展的量子计算所需的各种单元模块。在这里，我将首先回顾当前硅基量子计算领域所取得的进展，并且对于掺杂原子的系统进行着重介绍。进而，我们将介绍如何对掺杂原子系统的单电子和单原子核自旋进行有效的高保真度调控，并说明进行量子计算的算法实现方案。最后，我将介绍系列面向集成的思路和探索。

D06-02

最终交流类型：口头报告

A Foundation for Fully Electrically Controlled and Microwave-Coupled Quantum Bits : Ultrashallow,

Heavily Strained Quantum Wells

Yiwen Zhang*[1,2,3], Zonghu Li[3], Yuchen Zhou[4], Yuhui Ren[1,2], Jiahan Ke[1,2], Jiale Su[1,2], Yanpeng Song[5], Jun Deng[5], Yang Liu[4], Runze Zhang[4], Haiou Li[3,4], Baochuan Wang[3,4], Zhenhua Wu[1,2], Jun Luo[1,2], Zhenzhen Kong[1,2], Gang Cao[3,4], Guoping Guo[3,4], Chao Zhao[5], Guilei Wang[1,3,5]

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2. University of Chinese Academy of Sciences
3. Hefei National Laboratory, University of Science and Technology of China
4. CAS Key Laboratory of Quantum Information, University of Science and Technology of China
5. Beijing Superstring Academy of Memory Technology

Ge/SiGe heterostructure quantum well structures, utilizing Ge two-dimensional hole gas, have emerged as a promising avenue for the development of spin quantum bits, attributable to their low disorder and high mobility. This study focuses on the epitaxial growth of high-quality virtual substrates on 8-inch silicon wafers using reduced pressure chemical vapor deposition (RPCVD). By fine-tuning key parameters such as the thickness of the reverse gradient buffer layer and the Si1−xGex buffer layer, surface roughness was optimized. Strain modulation of dislocation dynamics enabled the creation of high-quality strained quantum wells, characterized by a density of stress accumulation points (DSAP) of 0.301/μm² and a surface RMS roughness of less than 3 nm. Ultimately, an ultrashallow, heavily strained, undoped quantum well was achieved, featuring a well depth of 15 nm, in-plane compressive strain (ε∥) of −1.19%, and a mobility of 3.382 × 10^5 cm^2/Vs. A novel characterization method for quantum wells was introduced, based on the defined DSAP. The combination of ultrashallow quantum well depth and increased compressive strain enhances the effective g factor (up to 8.3), positioning this structure as an ideal platform for fully electrically controlled and microwave-coupled quantum bits.

D06-07

最终交流类型：口头报告

Effect of Ge content in poly SiGe on WER under ADM solution

Weiran Li[1], Libin Jia[1], Yang Xu[1], Jiabao Sun[1], Huimin Ren[1], Dingting Han[1], Chaoyang Guan[1], Hongbo Sun[1], Guilei Wang[1], Chao Zhao*

1. Beijing Superstring Academy of Memory Technology

In this work, the effect of Ge concentration of polycrystalline (poly) SiGe on it’s wet etch rate (WER) under ADM (20:1 Ammonium hydroxide) solution was investigated. Firstly, An ALD titanium nitride (TiN) film was deposited on the surface of a P-type wafer as substrate, and poly SiGe(B-doped) was then deposited by a low pressure chemical vapor deposition process (LPCVD). In this deposition process, silane, germanane and borane were thermally decomposed at 420 ℃ to achieve the deposition of poly SiGe films. The Ge content of poly SiGe can be adjusted by changing the gas flow of germanane. TEM images show that, with the increased amount of Ge, larger grains has been observed in the film, which is because of the easier decomposition of germane than silane at 420 ℃ and higher deposition-rate. We also checked the wet etch rate (WER) of poly SiGe film with different Ge content using 20:1 ADM solution at 65 ℃. It was found that the WER under ADM solution decreased gradually with the raising Ge concentration, and the ADM solution could not etch poly SiGe with Ge content >60% in film. We also found that the etch rate is inversely proportional to the Ge content in the film. When Ge content is 17.6%, the etching rate can reach 2.4 nm/min. The WER of poly SiGe can’t reach the WER of undoped poly(about 50 nm/min) even at very low Ge content(2%), which is cause by boron in poly SiGe film and boron will decrease the WER of poly SiGe under ADM.

D06-08

最终交流类型：口头报告

硅基纳米隧穿场效应晶体管的噪声表征

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纳米级 TFET 兼具理论高效率和生产低成本两大优势，是晶体管研究的热点和前沿，但目前最为关键的问题是器件等比缩小导致的物理极限；此外，对器件内部载流子的产生、分离、传输、扩散等过程也要深入研究。噪声作为一种新的表征手段，能够快速无损的直接与材料及器件内部不同类型缺陷产生联系，可解决以上问题，且更加灵敏可靠。目前对纳米 TFET 噪声虽有大量研究，但主要以器件工作在沟道区的热噪声为主，而对器件中隧穿电流穿过势垒形成的散粒噪声研究甚少。因此，选择纳米 TFET 为研究对象，研究沟道区与栅、源、漏区噪声产生机理及缺陷形成原理，根据失效物理方法建立多噪声模型。

D06-09

最终交流类型：口头报告

Study on the etching method to optimize the Polycrystalline silicon profile smoothing and interlayer uniformity in lateral cavity with high aspect ratio multilayer structures

Yang Liu[1], Zehuan Hei[1], Xiaodong L[1], Jiao Jin[1], Xiao Shang[1], Tuo Xin[1], Zhonghua Jin[1], Chaoyang Guan[1], Baodong Han[1], Hongbo Sun[1], Shangbo Yang[1], Guilei Wang[1], Chao Zhao*

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In the preparation of oxide/ silicon nitride(O/N) stacked Structure for 3D device with high aspect ratio(HAR), it is necessary to fill the cavity formed by lateral etching with dummy materials. Due to the loading effect, the filler material is deposited thicker in the top layer and hole bottom, which causes deformation of the profile of the dummy material remain in the cavity and uniformity worse during the etching process. In this paper, we mainly investigated the effect of various etching methods on the profile smoothing and interlayer uniformity of the dummy material in the cavity. Polycrystalline silicon is used to fill 5 tiers of O/N-stack lateral dummy materials with HAR of 10:1. The O2 oxidized Polycrystalline silicon surface is applied to ensure that the break though step will open the top and bottom oxidized layer and protect the side wall Polycrystalline silicon. Then, the thick Polycrystalline silicon at the top and bottom was reduced to the same thickness as the sidewall by anisotropic etching in punch step. Finally, the Polycrystalline silicon at the top, bottom and sidewall was completely removed by wet method, and the dummy material in the cavity remained as designed. The etching method ensures the profile smoothing of Polycrystalline silicon in the cavity, and the uniformity of Polycrystalline silicon remain between layers is improved to 3%. The results provided a useful method for 3D device structure fabrication.

D06-10

最终交流类型：口头报告

提升高 K 氧化物介电性能的通用策略及其在晶体管的应用

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Vacuum-free, solution-processable high-κ-oxide dielectrics are considered to be a key element for emerging low-cost ffexible electronics. However, they usually suffer from low breakdown strength and

frequency-dependent capacitance, which limit their broader applications. Here, we report a universal way to improve solution-based high-κ oxide dielectric properties (e.g., Al2O3, ZrO2, Ga2O3, Sc2O3, Ho2O3, and Sm2O3) by sulfate incorporation. In-depth characterization shows that sulfate incorporation could reduce hydrogen and oxygen vacancy-related defects in high-κ oxides, thereby improving the dielectric performance. The optimized S-doped high-κ oxides show smooth surface (rms < 0.20 nm), low leakage current (□10−7 A/cm MV/cm), excellent dielectric breakdown strength (>10 MV/cm), and stable capacitance−frequency characteristics. Besides, oxide thin-fflm transistors based on these high-κ dielectrics exhibit excellent performance (e.g., mobility >20 cm2 V −1 s−1, on/o and hysteresis of □0.02 V). Finally, this work pro solution-based high-κ oxides for transistor circuitry.

D06-11

最终交流类型：口头报告

Research and fabricate of SiO2/SiN stacked structure with low hydrogen content and low stress

Xin Zhang[1], Tielu Liu[1], Chao Tian[1], Jiabao Sun[1], Zhao Chao[1,*]

1. Beijing Superstring Academy of Memory Technology

The foundation of IGZO thin film transistor construction is that it requires low single-layer film stress, low wafer warpage and low hydrogen(H) content in the stacked structure. This work is to deposit SiO2/SiN stacked on 12-inch wafers based on the PECVD deposition machine, the stacked structure scheme of 5tire SiN(50nm)/SiO2(50nm)+SiN(50nm) was explored to reduce the film stress, wafer warpage and H content of the film. SiO2/ SiN film layers prepared by 400℃ PECVD SiO2 and 550℃ PECVD SiN deposition machines, and the ON stacked structure was built alternately. Compared with the stacked structure constructed by 550℃ SiO2/ SiN integrated PECVD deposition machines, The stress of SiN film decreases from 307Mpa to ~250MPa, and the stress of SiO2 film decreases from -354MPa to -250MPa, and the stress gap between the single-layer films decreases significantly, making the warping of the layers offset each other. At the same time, the H content in SiN is reduced from 21% to about 6%, which meets the requirements of IGZO thin film transistors for SiO2/ SiN stack. 800/900/1000℃ RTP treatment was applied to the stacked structure deposited by PECVD at 400℃ SiO2 and 550℃ SiN, which improved the slight bending of ~2o in the suspended monolayer film after lateral etch, and the uneven etching between monolayer films due to different deposition temperatures, the difference is ~11nm. By separately controlling and optimizing the SiO2/SiN thin film lamination structure, the film stress, wafer warpage and H content of the stacked structure are effectively reduced, and the etch profile is improved by RTP treatment, providing data support for multi-layer film stacking with low stress and low H content.

D06-I12

最终交流类型：邀请报告

高能效铁电存内计算器件与集成

于志浩[1]，宁宏凯[2]，温恒迪[2]，傅玉祥[3]，王欣然[2,3]

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为满足大数据时代中不断增长的计算需求，人工智能需要从云端向边缘转移。非易失存计算（IMC）是边缘智能（EI）最高能效方案，但由于现有存储技术的性能限制，具备高能效的原位训练和推理、无索

引的原位稀疏化一直是极具挑战性的领域。我们报道了一种基于铁电场效应晶体管（FeFET）和原子层厚度的 MoS2 沟道硬件解决方案：通过设计存内计算单元架构，开发软硬件协同的算法，实现了具备本地化训练和推理、存内稀疏能量的通用 IMC 体系，基于此搭建了全硬件神经网络，在非线性定位、图像识别等计算任务中展示显著的能效优势，为边缘端计算提供新的解决方案。

D06-I13

最终交流类型：邀请报告

Atomic-level observation of Hf0.5Zr0.5O2 thin films

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HfO2-based ferroelectric (FE) materials have attracted extensive attention in the research of next-generation nonvolatile memories and logic devices due to their superior scaling property and compatibility with CMOS process. However, HfO2 system has a variety of phase structures, and the orthorhombic (o-) FE phase is not thermodynamically stable, which bring many challenges to the mechanism research. For example, atomic layer deposited Hf0.5Zr0.5O2 (HZO) thin films need to undergo rapid thermal annealing (RTA) process with clamping to produce ferroelectricity. Therefore, how does the FE o-phase form, and how its structure evolves with the electric field operation, are all topics worth discussing.

In this talk, spherical aberration corrected transmission electron microscope (Cs-TEM) as the main research techniques for unveiling the atomic-level structures of HZO thin films prepared by ALD, and the main content is as follows:

1. The dynamic process of o-phase emergence during RTA in polycrystalline HZO ferroelectric film (Figure 1) was directly visualized though in-situ Cs-TEM technique.

2. The dynamic atomic scale structural evolution from centrosymmetric tetragonal (t-) phase to FE o-phase under electric field was visualization.

3. Atomic-scale characterization of lattice dislocation and monoclinic (m-) formation by martensitic-like transformation of HZO thin films during fatigue.

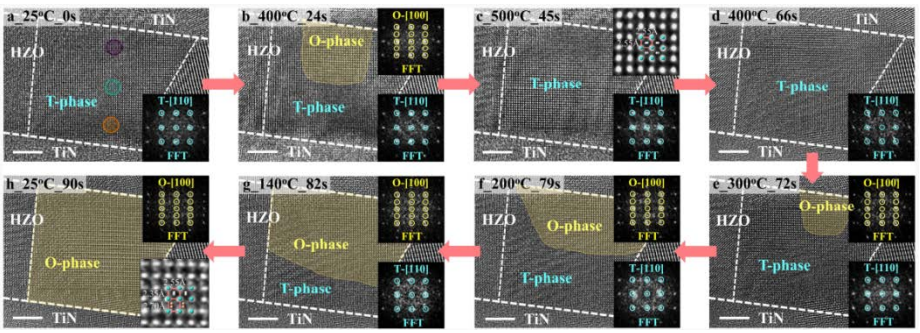

Figure 1. HRTEM images show the o-phase emergence from t-structure with in-situ RTA in TEM: (a) room temperature→(b) 400oC→(c) 500oC→(d) 400oC→(e) 300oC→(f) 200oC→(g) 140oC→(h) back to room temperature. The insets show the FFT patterns of each t- or o-region, clearly demonstrating the t- and o-structures.

Bar = 3 nm.

D06-I14

最终交流类型：邀请报告

Breaking the Switching Endurance Limits of Phase Change Memory

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In the realm of emerging storage technology, phase change memory (PCM) has been regarded as a prospective next generation solution to transform the established paradigms in traditional storage architecture owing to its attributes of good scalability, non-volatility, and fast speed. However, the high switching power and limited cyclic switching endurance remain a critical challenge of PCM technology as storage class memory. In this work the en- durance performance of the mushroom-type PCM devices adopting a self-confined structure and carbon-doped GeSbTe (CGST) material is extended to more than 1.1E11 cycles by the mitigation of over-programming effect. The over-programming of the PCM cell induced by excessive RESET current gives rise to the recrystallization of the active phase change volume which accelerates the migration of the segregated carbon atoms toward bottom electrode and leads to the resultant contraction of the switching volume. Moreover, the cyclic switching operation exacerbates the over-programming effect which intensifies the carbon atom segregation with denser cluster surrounding the active region and ultimately causes the RESET-stuck failure. The self-confined structure enables efficient heating by relocating the melt-quench region away from the interface to the dielectric layer. It is therefore significantly reduces the energy required for RESET switching which, consequently, mitigating the over-programming effect. The endurance performance of the PCM cell can be further extended through additional optimization both in device structure and programming scheme. This work paves a way towards storage class memory employing PCM devices that feature both ultralong cyclability and high thermal stability without adding the process loading.

D06-I15

最终交流类型：邀请报告

低功耗自旋电子存储器关键材料研究

曹凯华[1,2]，史可文[1]，蔡文龙[1]，朱道乾[1]，张和[1]，王碧[1]，王昭昊[1]，赵巍胜[1]

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在大数据时代，传统冯·诺依曼架构在面对海量数据时出现了存储和功耗瓶颈。随着非易失存储器的快速发展，高写入速度、低功耗的磁随机存储器（MRAM）为“存算一体”架构的实现带来了新的曙光。本研究围绕自旋转移矩磁随机存储器（STT-MRAM）、自旋轨道矩磁随机存储器（SOT-MRAM）和反铁磁基随机存储器（ARAM）三款最具潜力的自旋存储器关键材料开展研究，通过氧化镁/铁磁/重金属的材料界面工程调控界面磁各向异性能、自旋相关散射态密度分布，在单原子层的重金属钨作为间隔层和双界面组成的垂直磁各向异性膜堆结构中，隧穿磁阻比率值达到了 249%，电阻面积矢量积则低至 7 Ω·μm2。通过元素掺入实现调控β晶相钨厚度窗口，结合垫层、叠层和插层的材料工程技术，在钨基薄膜电极中获得了高达 0.58 类阻尼矩效率，实现了接近 48%的器件翻转功耗降低，并在 1Kb SOT-MRAM 阵列级中通过 125℃高温和 3 倍操作电压双重加速老化观测到元素扩散机理导致的器件失效。通过引入反铁磁材料到 SOT-MRAM 结构中，将信息存储在反铁磁磁序状态里，隧穿磁阻比率值达到了 80%，实现了基于 SOT 效

应的 0.8ns 全电学反铁磁磁序状态操控。本系列研究为 STT-MRAM、SOT-MRAM 及 ARAM 芯片技术量产，提供了关键材料技术储备，有望推动自旋存储器技术在低功耗、高可靠应用场景的芯片工程化开发。

D06-16

最终交流类型：口头报告

低延时、高密度 InGeSbTe 相变存储芯片研究

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3D Cross Point 结构是实现高密度低延迟存储级内存的有效途径之一，通过堆叠存储单元和选通器件（1S1R），相变存储器的位密度得到了进一步提高[1]。然而，堆叠相变材料和选通材料的工艺复杂性使得进一步增加堆叠层数的挑战急剧升高。为了降低工艺集成难度和成本，从材料工程的角度开发具有良好工艺兼容性和多级存储潜力的新型存储材料是提升相变存储器集成密度和存取速度的有效途径。多级存储单元（Multiple Level Cell, MLC）是提高集成位密度的有效方法，但当前的 MLC 技术需要反复迭代器件编程参数和额外的读写电路，这不适合对低延迟操作要求极高的存储级内存的应用需求[2,3]。最近的研究表明，使用 1S1R 结构可以实现不需验证操作的 MLC 编程方案，但仍需要在重新编程前进行初始化操作[4]。因此，未来经济高效的存储级内存应用仍需要进一步改善 MLC 技术。

本研究提出了一种通过单脉冲编程实现四级电阻态的相变存储器，即仅使用单次电学脉冲编程即可实现具有低延时、高密度存储潜力的 MLC 技术。本研究使用六种操作脉冲实现了四级 MLC 技术中的任意一个状态向其余三个状态的转变。通过优选的 InGeSbTe 相变材料组分和纳米刀片电极加热结构，四级相变存储器具有两个数量级以上的读取窗口和百纳秒级别的操作速度。这为单脉冲 MLC 编程技术在器件阵列中的应用提供了可行性。通过可编程配置的读写电路，本研究设计了四级相变存储器中各级状态之间转变的操作脉冲。同时还探究了阵列级 4Mb 多级相变存储器的四级电阻态循环擦写寿命和疲劳擦写操作后各级电阻的漂移行为。

最终结果显示，本文提出的单脉冲编程方法在低延时、高密度的相变存储器中实现了超过 1E7 次的循环擦写寿命。在经历 1E7 次疲劳擦写后，典型的电阻读取窗口仍超过了 1 个数量级。该单脉冲编程的多级相变存储器表现出良好的电阻稳定性，编程后经过 120 个小时的电阻漂移测试，其编程误码率约为 5E-4，结合 8 纠 1 纠错码，可以满足芯片的高密度应用需求。

D06-17

最终交流类型：口头报告

高热稳定性、高可靠 C-In-Sb-Te 相变材料研究

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相变存储器（PCM）在汽车电子等高温环境中的应用需求对相变材料的热稳定性和可靠性带来了巨大挑战。本研究基于由匹配八面体 In-Te 和 Sb-Te 基元构成的稳定相变材料，通过掺入碳原子实现三维限定相变材料晶粒尺寸，获得了高热稳定性、高速的新型 C-In-Sb-Te 相变材料。该材料十年数据保持力温度为 160°C，相应存储器件的阻值开关比超过 2 个数量级，擦写速度低至 6ns，循环擦写的疲劳寿命超过 1E6 次。同时器件单元在经过 400°C 高温热处理后，仍可循环操作超过 5E5 次，表现出高可靠存储的潜力。使

用球差透射电镜和电子能量损失谱（EELS）分析了高温退火后的 C-In-Sb-Te 相变材料微观结构，发现 C 原子限制了晶粒生长，形成了晶粒尺寸约 10 nm 左右的晶态结构；同时没有观察到八面体基元的失配现象，In、Sb、Te 元素分布均匀。本研究表明在稳定匹配八面体基元构成的相变材料中引入 C 原子可有效限定晶粒尺寸和实现均一的晶粒尺寸分布；C-In-Sb-Te 相变材料有望用于针对高温应用场景需求的高可靠 PCM 芯片工程化开发。

D06-18

最终交流类型：口头报告

基于非晶氧化镓的低功耗阻变存储器研究

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氧化镓材料介电常数较高，绝缘性能好，同时非晶氧化镓内部含有丰富的氧空位，是一种非常理想的阻变材料。基于此，我们制备了单层非晶氧化镓的单双极共存的阻变存储器，单双极性下均有 104 的开关比，且在 104 s 下高低阻态均能保持稳定。另外，我们还制备了结构为 Ag/TiOxNy/Ga2O3/Pt 的双层阻变存储器，器件具有较低的置位电压（0.17 V）和复位电压（-0.057V）以及极低的功耗（21.7 μW, 0.17 μW）。同时器件在不同光照强度下（365 nm）可以实现八种电导状态，展现了良好的光存储特性，有望实现多级存储。

D06-19

最终交流类型：口头报告

Effect of High Temperature Furnace Anneal to Element Diffusion in SiO2/Si3N4 Stacks

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The choice of multilayer stack plays an important role in the 3D DRAM architecture realization. Si-SiGe, SiO2-Si3N4(ON) and other potential stack materials are well known at present. Among them, ON stack is a relatively ideal stack material because of its simple preparation process and mature application in the field of 3D NAND.

Recently, we found that after vertical etch 5 tiers of ON stacks and then lateral etch SiO2, the remaining SiO2 layers show a slope profile with wide at top and narrow at bottom. Moreover, the suspended Si3N4 generated after lateral etch show a slightly bending. Aiming at this phenomenon, we analyze the possible mechanism is that the different thermal treatment on the upper and lower surfaces of SiO2 during the stack preparation process makes the element diffusion uneven, resulting in a slope-type profile after lateral etch. The bending of Si3N4 may cause by the stress release after lateral etch SiO2.

According to this presumption, 600/700/800°C furnace anneal for 30 min in N2 atmosphere of ON stacks was added before etch, element diffusion and nitride bending after anneal was then explored. Compared with non-anneal ON stacks, the content of N in SiO2 increases from 7E18 to 1E19, and the distribution of N is more uniform with temperature increase. Furthermore, H content in the SiO2 layers also decreases from 2E20 to 1.5E20, which is benefit to channel stability. The same etch process was then performed on the post annealed ON stacks, slope-type profile was disappeared and the bending of Si3N4 was significantly improved. These results prove the correctness of the previous inference that the uneven diffusion of N leads to the formation of slope-type profile, and high temperature anneal can decrease intrinsic stress of film, which is beneficial for the 3D DRAM generation

in the future.

D06-20

最终交流类型：口头报告

Radical etching of staircase metal line in 3D DRAM

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In 3D DRAM, staircase metal line is usually use as the electrical contact between bit line and contact line. Tranditional plasma etch is unsuitable because of staircase matel line preparation need etch surface and side wall simultaneously. Matel line atomic layer deposition（ALD）in staircase pocket can't avoid seam profile, which will lead to uncontrolled matel void introduced by wet etching. In this paper, the radical etching of staircase titanium nitride (TiN) metal line preparation is investigated. For radical etching, the incoming species are neutral radicals. When etching TiN with CF4, the etching rate (ER) is same in each direction and strongly related to the reaction area. When the surface TiN is fully removed, the ER of pocket TiN will increase from 14 nm/min to 30 nm/min. The bias power can cause the secondary ionization of the neutral particle, which can change the ER ratio in vertical and lateral direction. In the TiN radical etching with SF6, the vertical and lateral ratio of ER can be greater than 10 by adding bias power, which can reduce TiN loss in staircase pocket. Such process for forming staircase metal line shows great potential in 3D DRAM fabrication.

D06-21

最终交流类型：口头报告

铁电向列相液晶中的半整数涡旋对及其动力学研究

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凝聚态系统中，连续性对称破缺系统中产生的局部取向不连续区域被称为拓扑缺陷，这些缺陷广泛存在于铁电材料，铁磁材料，液晶材料等物态系统中。这些拓扑缺陷在材料系统中具有特别的光，电，磁，机械和拓扑性质，在新型电子器件的开发，对凝聚态物理系统的理解等具有重要的意义。我们报告了通过一种普适性通过在 NF 相中引入阳离子聚合物的方法，发现了一个半整数涡旋弦的极性拓扑结构。从实验上探索了这些缺陷对的形成和结构，证明了这些缺陷对的形成依赖于铁电性和挠曲电性引起的对称破缺和电荷选择。高分子量的阳离子掺杂剂实验证实是聚合物形成弦结构正电荷核心的关键。通过观察在平面直流电场下这些孤子状缺陷对结构的电泳行为，探究了缺陷对的可控动力学和它们的合并行为，并通过具有静电力和粘滞阻力的力平衡模型描述了它们的运动行为。此外，这些缺陷对展示了在电场反转时的两种截然不同的反转行为，为研究极性拓扑缺陷的反转动力学提供了实验平台。这些由掺杂剂引起的缺陷对可能为在 XY 模型中研究极性拓扑及其动力学，可视化物质运输提供了一种新的实用方法，并可能增加对铁电向列相新的理解。

D06-I22

最终交流类型：邀请报告

石墨烯与基底相互作用的原子模拟研究

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石墨烯具有优异的力学、电学、热力学和光学特性，第一性原理计算等原子模拟手段可以从电子和原子尺度探究这些优异特性的起源和调控手段。通过原子模拟方法研究了石墨烯与 Ge、Ru、Ir 和 Cu 等界面的相互作用，给出了石墨烯具有优异摩擦特性的根源。以扭转石墨烯为研究对象，给出了扭转石墨烯垂直电流随扭转角演化的完整物理图像和扭转石墨烯“多米诺骨牌形式”堆垛转变的原子层次机理。最后，通过原子模拟证明了覆盖石墨烯的极性 NaCl 基底能够远程调控 CsPbBr3 薄膜的外延生长，并依据该机制成功制备出了低位错密度的高质量 CsPbBr3 薄膜。

D06-I23

最终交流类型：邀请报告

“水上漂”的二维碘化物光电材料

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传统的液相方法在合成和加工具有宏观尺寸和极薄厚度材料方面缺乏精确控制。水界面在催化许多化学反应中是无处不在且独特的。然而，与水界面相关的二维（2D）材料的研究仍然显著有限。在这里，我们报告了在水-空气界面上生长毫米级 2D PbI2 单晶的方法。这是基于一种称为固有离子特异性偏好的新型生长机制，即碘离子和铅离子分别倾向于停留在水-空气界面和体积水中。碘离子在水-空气界面的自发积聚和平面排列导致了 PbI2 以及 SnI2、GeI2 和 CdI2 的独特结晶。特别是，PbI2 晶体可以定制成特定厚度，并进一步转化为毫米级单层至少数层的钙钛矿材料。此外，我们开发了基于水的技术，包括水浸泡、旋涂、水蚀刻和水流辅助转移，用于回收、稀释、图案化和定位 PbI2，随后是钙钛矿材料。我们的水界面介导的合成和加工方法标志着在实现功能材料及其集成器件的简单、具有成本效益和节能生产方面取得了重大进展。

D06-I24

最终交流类型：邀请报告

离子束沉积技术及应用

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离子束沉积（IBD）技术已成为先进材料科学中的关键方法，能够精确控制薄膜的厚度、成分、覆盖率和微观结构。本次演讲将深入探讨离子束沉积的基本原理，阐明其区别于物理气相沉积（PVD）等其他沉积技术的独特机制。我们将详细探讨 IBD 的关键方面，包括溅射离子源、辅助离子源、栅网、特殊构造的载台以及影响沉积速率的关键因素等。将重点介绍 IBD 在生产高质量薄膜方面的多功能性，特别是其在实现优异的薄膜均匀性、覆盖性、密度、表面粗糙度、电阻率和选择性沉积方面的卓越能力。我们将探讨 IBD 在原子级精确调控材料特性方面的能力，使其能够制造具有定制光学、电学和机械特性的薄膜。同时，还将强调 IBD 与多种基材的广泛兼容性，包括半导体、介电材料和金属。此外，我们将探讨 IBD 在各个行业中的广泛应用，展示其在半导体、光学涂层和磁性薄膜生产中的重要影响。具体案例研究将展示离子束技术如何在微电子领域实现突破，例如其在制造超低电阻率的氮化钛（TiN）和钨（W）材料方面的应用。

D06-25

最终交流类型：口头报告

高迁移率稀土掺杂氧化物半导体材料及应用

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2004 年，日本东京工业大学的 Hosono 教授发明了用于薄膜晶体管（TFT）的非晶态氧化物半导体材料 InGaZnO4（IGZO），高 Ga 掺杂解决了关态电流高、TFT 器件难以关断的问题，使其成功应用于平板显示。但是，其面临迁移率相对较低、在负栅偏压+光+热应力（NBITS）下的阈值电压漂移问题。针对上述迁移率较低、NBITS 稳定性差的基础科学问题，本文研究了稀土离子的电荷转移跃迁对氧化物半导体的光稳定性的改善作用。研究表明：四价稀土离子（ 如 Pr4+和 Tb4+）的电荷转移跃迁能将入射光下转换成无辐射跃迁（从|Ln4f n—O2p6>态转移至|Ln4f n+1—O2p5>），能大幅改善氧化物 TFT 光热稳定性。

D06-26

最终交流类型：口头报告

基于离子束剥离技术的功能性 GaN 异质集成衬底材料

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宽禁带半导体 GaN 材料具有禁带宽度大、临界击穿场强高、电子饱和漂移速度高等特点，适合制作高频率、大功率、集成化的射频电子器件，在 5G 通信、雷达卫星、航空航天等领域也有着很大的应用前景。随着氮化镓材料的发展，氮化镓单片集成的需求日益增长，传统异质外延生长技术仍面临晶格失配、晶型失配、反相畴、需要较厚的缓冲层等问题。与异质外延生长技术相比，离子束剥离技术是一种更为灵活的异质集成材料制备方法，通过离子注入从单晶晶圆上剥离晶圆级单晶薄膜，并通过异质键合的方法将其与所需要的异质衬底进行集成。本工作已成功实现 2-4 英寸 GaN 单晶薄膜与 Si(100)衬底的集成，形成 GaNOI 结构（GaN-on-SiO2/Si(100)），以满足 GaN 基器件和 Si 基 CMOS 集成的需求。针对 GaN 大功率器件的散热需求，我们也开展了将 GaN 单晶薄膜与高导热衬底如 SiC、金刚石等材料集成的相关工作，目前已实现了 2-4 英寸无缓冲层 GaN/SiC 异质集成衬底，以及小尺寸 GaN/金刚石异质集成衬底材料。材料表征结果表明，所制备的 GaN 单晶薄膜具有很好的单晶质量，单晶薄膜厚度约为 500nm，(002)面 XRD 半高宽为 50.4arcsec，表面粗糙度 Rq 约为 0.5nm。

D06-27

最终交流类型：口头报告

High-Precision Characterization of Dislocations in 4H-SiC Wafer Using Synchrotron Radiation X-ray Topography

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4. CEC compound Semiconductor Co.,Ltd.

High-precision topography of silicon carbide (SiC) wafers has been achieved through the use of

grazing-incidence topography (GIT), synchrotron radiation X-ray plane-wave topography (SXPWT). These techniques allow for the observation of the distribution of threading screw dislocations (TSDs), threading mixed dislocations (TMDs), threading edge dislocations (TEDs), and basal plane dislocations (BPDs), which distribute from 100 nm to 10 μm under the surface. At the Shanghai Synchrotron Radiation Facility (SSRF) BL09B beamline, GIT measuring enables the characterization of near-surface dislocations of a 4-inch 4H-SiC wafer within one minute. By combining SXPWT with rocking curve imaging (RCI), it is possible to quantitatively measure the lattice distortion Δd/d caused by dislocations with a precision ranging from 1E-7 to 1E-8. Moreover, section topography combing with step-by-step scanning allows for the reconstruction of a complete three-dimensional defect distribution map of the SiC wafer.

D06-28

最终交流类型：口头报告

Assessing the impact of defects on performances of Ga2O3 photodetector via photoinduced current transient spectroscopy

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1. Xidian University

Heteroepitaxy is often used to grow films for solar-blind photodetectors like sputtering, Mist-CVD, and MOCVD, due to the low cost of substrate and fabrication. Due to low crystalline quality, the films are resistive. High responsivity and slow response due to persistent photoconductivity are the typical features. Several compensated defects are suspected to account for the resistive and response feature within the bandgap and can be reduced by annealing. However, the corresponding defect level, capture cross-section, and physical origin, have not been revealed yet, which causes high responsivity but a long rise time, hindering the advances of Ga2O3-based solar blind detectors.

The technique of monitoring the transient of junction capacitance, namely, deep-level transient spectroscopy (DLTS), is a powerful tool to characterize deep levels. However, for the application of solar blind photodetector, highly resistive Ga2O3 is often used to form Ohmic or Schottky metal-semiconductor-metal (MSM) photoconductor structure. Here DLTS is not applicable due to small junction capacitance and difficulties in injecting free carriers by voltage pulse. Alternatively, photo-induced current transient spectroscopy (PICTS) is used to characterize trap levels in highly resistive semiconductors.

In this work, representative highly resistive Ga2O3 epilayers were grown on sapphire by metal-organic chemical vapor deposition. For the photodetector, two interdigital electrodes of Ti/Au were deposited by electron-beam evaporation, and ohmic contact was formed after annealing under a nitrogen atmosphere. The representative dark and light I-V curves, spectral response, and I-t response were measured using a Keithley 2450 source meter with a 254 nm LED. The PICTS were carried out in a home-built setup using Zurich Instruments MFLI lock-in Amplifier. The data analysis of PICTS is still ongoing. This work will provide insight into defect identification and modulation in the Ga2O3 solar-blind photodetector field.

D06-29

最终交流类型：口头报告

功能性蓝相液晶材料

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蓝相液晶因其独特的三维自组装超结构、多重外界刺激响应性、实时可重构性和优异的光学性能等吸引了研究者的广泛关注，在柔性光电器件中具有重大应用潜力。然而迄今为止，仍然缺乏对蓝相液晶多级结构和相变过程的实时观测，对功能特性的发掘仍然不足，从而限制了其实际应用发展。我们通过对蓝相液晶自组装过程的研究，引入可聚合液晶单体和非液晶性单体，实现了大面积、高质量、自支撑的多色单畴蓝相液晶光子晶体薄膜的制备；进一步通过合适的聚合物稳定体系扩宽了蓝相液晶的温域（-190~310 ℃），并结合同步辐射、透射电镜等多手段详细研究了其相转变过程；利用蓝相液晶的刺激响应性研究了蓝相液晶光子晶体薄膜在形状记忆聚合物方面的应用；结合喷墨打印技术，发展了多色精美的蓝相液晶“活”图案；基于蓝相液晶谐振腔实现了高品质蓝相液晶激光，并进一步将其激光温域扩宽至超过 400 ℃（-180~240 ℃）。这些工作极大的促进了功能性蓝相液晶在显示、防伪、激光等领域的应用拓展。

D06-30

最终交流类型：口头报告

GaN 纳米复合 Sn-Ag-Cu 无铅钎料焊点的微观组织及性能研究

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通过机械混合法制备不同质量分数（0wt%，0.20wt%，0.40wt%，0.60wt%，0.80wt%）纳米 GaN 颗粒复合 Sn-3.0Ag-0.5Cu 无铅钎料。采用回流炉制备焊点并进行了 170℃的不同时长的高温存储模拟实验。研究了不同含量的 GaN 对 Sn-3.0Ag-0.5Cu 无铅钎料的熔化特性，润湿性，金属间化合物（IMC）生长特性和剪切性能的影响。结果表明，添加 GaN 对 SAC305 的熔点没有显著影响，适量添加 GaN 可以改善 Sn-3.0Ag-0.5Cu 的润湿性，在含量为 0.40wt%时润湿性最佳，对比 Sn-3.0Ag-0.5Cu 降低了 61.5%。添加 GaN 可以抑制 IMC 层的生长，随着等温时效时间的增加，IMC 层逐渐增厚，其生长行为受扩散控制，其扩散系数最低为 1.453×10-15m2/s。复合钎料的显微硬度和剪切性能均得到明显提升。综上所述，新型复合钎料 SAC305-0.4GaN 表现较优。

D06-31

最终交流类型：口头报告

Machine learning assisted high-throughput design of high-performance and low-power 2D diamane short-channel transistors

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Two-dimensional semiconductors are regarded as important candidate to replace silicon in the post-Moore era for high-density integrated circuit (IC) manufacturing, due to their unique electronic properties, excellent gate control capability, and free of surface dangling bonds. Based on theoretical calculations, this study systematically evaluates the performance of short-channel field-effect transistors with ultra-wide bandgap semiconductor two-dimensional (2D) diamane as channel materials at sub-5 nm nodes. In high-performance scenarios, the on-state current of the transistor at the 5 nm node is as high as 2908 μA/μm, the subthreshold swing (SS) is only 70 mV/dec, and the key parameters such as power delay product and energy delay product are far lower than the requirements of the IRDS2028 standard. The excellent performance is attributed to the ultra-high carrier mobility and state density at the band edge. To improve the carrier injection efficiency between the metal electrodes and transistor source/drain regions, a physically interpretable model is established to map the material parameters of transistor channel and source electrodes to the device parameters such as device tunneling

resistance and longitudinal/lateral Schottky barrier resistance, through constructing ARANet and DARNet machine learning models, and a low-contact electrode screening process with high accuracy and high efficiency is developed. To further reduce the power consumption of 2D diamane transistors, high-throughput calculations are used to screen electrode materials with reduced state density distribution characteristics near the Fermi level, and a low-power transistor with a subthreshold swing below 60 mV/dec is realized by constructing a cold source structure. At the same time, the on-state current is much higher than the IRDS2028 standard. These works provide new methods and ideas for the research and development of 2D semiconductor transistors, and demonstrate their great potential in the next generation of high-density ICs.

D06-32

最终交流类型：口头报告

Investigation of Silicon Oxide/Tungsten/Titanium Nitride Stack Multi-step Etching

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1. Beijing Superstring Academy of Memory Technology

Silicon Oxide, Tungsten, Titanium Nitride are common materials in semiconductor device fabrication areas. Silicon Oxide as dielectric layer, Tungsten as conductive layer, Titanium Nitride as adhesion layer. According to the characteristics of the material and the pattern requirements, Silicon Oxide, Tungsten, Titanium Nitride need use different plasma source etching. The periodic stacked film etching is a key enabler of 3D device manufacturing, such as Silicon Oxide/silicon nitride(ON) periodic stacked film etching, Silicon Oxide/polycrystalline silicon(OP) periodic stacked film etching. However, few scholars have studied dielectric material/conductive material periodic stacked film etching. This paper investigates a silicon oxide/tungsten/titanium nitride(OWT) periodic stack etching in multiple etching steps. Because of the chemical reaction mechanism differences for various materials, the profile of the sidewall of the pattern is always some issue, such as top corner sharp, sidewall angle not vertical enough. This paper adopts O2/C4F6/Ar gases etching Silicon Oxide, adopts Cl2/NF3/Ar gases etching Tungsten and Titanium Nitride, Thus form Silicon Oxide, Tungsten, Titanium Nitride (OWT) periodic stacked sub-100nm holes. By tailoring the gas ratio, power, pressure, plasma distribution and ion bombardment strength, formed a smooth sidewall with an excellent vertical profile greater than 88°. Dielectric material/conductive material periodic stacked film etching sub-100nm holes is a key process of 3D DRAM vertical transistor manufacturing, can directly form a vertical source drain structure, Further formation channel all around structure. In this paper, OWT/OWT periodic stacked film etching is studied and an effective solution is provided.

D06-33

最终交流类型：口头报告

特殊结构单臂碳纳米管热导率的分子动力学模拟

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1. 贵州大学

采用非平衡分子动力学（NEMD）中的 Müller-Plathe 法，本研究探讨了特殊结构对单壁碳纳米管热导率的影响。我们将扶手椅型碳纳米管和锯齿型碳纳米管作为一组进行比较。通过理论计算，遍历整数从 1 至 135，成功筛选出 20 组单壁碳纳米管的对照模型，使得每组模型的管径误差均小于 0.1 埃，管长误差均为 0.0585 埃。在管长较短时，声子处于完全的弹道运输阶段，显示出管径和管长对两种结构碳纳米管的热导率影响甚微，故可认为热导率主要由碳纳米管的结构决定。

结果显示，在这 20 组对照组中，整体而言，扶手椅型碳纳米管的热导率普遍高于锯齿型碳纳米管的热导率。在管长较短时，小管径的结构效应不明显，此时结构对热导率的影响不大，然而，大管径的结构效应更为显著，导致两种结构的热导率差值有所增大。总体上，扶手椅型碳纳米管的热导率普遍超过了锯齿型碳纳米管。随着管长的增加，碳纳米管的热导率也随之增加，结构效应也变得更加显著和稳定，并且扶手椅型单壁碳纳米管的表现相较于锯齿型更为稳定。

D06-34

最终交流类型：口头报告

Polycrystalline silicon removal combining dry etching and wet etching process for 3D multilayer device fabrication

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1. Beijing Superstring Academy of Memory Technology

Polycrystalline silicon (Poly Si) is generally regarded as structure material and dummy material in 3D multilayer structure semiconductor manufacturing. The selective removal of Poly Si is therefore an essential process for 3D device fabrication, which requires the combination of patterning and deep hole etching. In this work, we developed a Poly Si removal method combining dry etching and wet etching steps for hole structure in multilayer device application. The hole was filled with Poly Si surrounded by 5nm SiO2 liner, which cannot be broken through during the Poly Si removal. The formed structure was then covered by Silicon Oxide (SiO2) and Silicon Nitride (Si3N4) hard mask layer on the top. It was found that the C & F elements based etching plasma for hard mask opening would form a Si/O/F blocking layer, preventing HF and ADM wet treatment to remove Poly Si. Therefore, it was difficult to fully remove Poly Si by dry or wet etching method alone, and a combined process of dry and wet etching was introduced. First, etching plasma generated from C and F based gas was selected for hard mask opening, followed by Cl2/HBr based plasma to remove a part of Poly Si. It was Proved by TEM result that the Poly Si surface etched by Cl2/HBr based plasma was free of blocking layer. Then O2/H2/N2 plasma and HF wet treatment to remove etching byproduct and native silicon oxide forming on top of exposed Poly Si, separately. The dry etching front stopped at 50nm above the SiO2 liner, which was at the bottom of Poly Si, to avoid substrate damage, and Ammonia Deionized water Mixture (ADM) wet etching was found capable of removing the remained Poly Si without damaging other material layers.

D06-35

最终交流类型：口头报告

水溶液作为溶剂实现铅基/无铅钙钛矿纳米晶绿色高效制备

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金属卤素钙钛矿纳米晶在光电领域具有广泛的应用前景。然而，绿色制备钙钛矿纳米晶一直是一个挑战。传统的制备钙钛矿纳米晶的方法中都包含有毒溶剂的使用，对环境和其产业化造成了严重威胁。 本报告展示用水溶液代替有毒溶剂来实现钙钛矿纳米晶的绿色制备。 研究表明，纳米晶的尺寸和发光波长可以通过超声时间和配体比例调节。 更重要的是，此绿色方法制备的钙钛矿纳米晶比传统方法制备的具有更高稳定性。这项研究为绿色高效制备金属卤素钙钛矿纳米晶提供了新思路，有望为进一步实现金属卤素钙钛矿纳米晶的产业化提供关键技术支撑。

D06-36

最终交流类型：口头报告

Research of UV cure effect on PEALD SiN WER in nonplanar structure

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1. Beijing Superstring Academy of Memory Technology

In some semiconductor manufacturing processes, there are strict controls on the thermal budget. With the high energy excitation of plasma, high-quality films can be deposited by traditional PEALD at lower temperatures. For example, the SiN film deposited at 350°C by PEALD tool can guarantee a low (<2.2nm/min@30:1 HF) WER(wet etch rate) in the planar structure even with H2. However, when it is applied to non-planar structures, due to the directivity of the plasma generation method (especially CCP), induce limited motion in horizontal, it is difficult to achieve a low HF-based solution etch rate on the premise of ensuring film high conformality everywhere in the non-planar structures. Through investigation, we found that the concentration of H will directly affect the etching rate of SiN film in HF-based solution. With the help of low temperature anneal after deposition, for example, UV cure can reduce the concentration of H in SiN film which can ensure both the thermal budget and high step coverage, so as to achieve a low HF acid WER. We investigated the effects of different UV cure time 1 min/3min/5min on film shrinkage and @ 30:1 DHF WER. Due to the limited transmission of UV wavelengths, the effect of UV cure on SiN film weakened as layers increase. With the increase of UV cure time, the shrinkage of PEALD SiN film showed a little trend up and then saturation, while WER shows trend down and then saturation. For UV cure 5min, the PEALD SiN film WER can be reduced by 30% on average under the target structure(ON stack, and SiO recess). And different locations(pocket inner and outer) of the structure, SiN film has a little different performance which caused by the CCP PEALD deposition. And this result can be potentially used in the scenario: WET selectively etch SiO and SiN in complex structure with HF-based solution and thermal budget constrains.

D06-P01

最终交流类型：墙报

The role of glass forming ability on switch endurance in Sb-Se chalcogenide amorphous

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Ovonic threshold switching (OTS) selector with the advantage of 4F2 density is crucial for integration with 3D nonvolatile memories. However, the reasons affecting the critical endurance performance of the devices remain unknown. Here, we screen arsenic-free Sb-Se OTS selectors to explore the correlation between the glass formation ability (GFA) and fatigue performance of the devices. The screened Sb2Se3 binary alloy consists of the fastest phase-transitioning elements, antimony and selenium, and offers the strongest glass-forming ability in a range of combinations, presents excellent OTS performance. The measured leakage current is 5 nA, on-state current exceeds 1 mA, and operation speed is under 10 ns. The endurance performance is also favorable. These findings reveal the strong influence of GFA on device performance and help in the design of high-end durable arsenic-free OTS selectors.

D06-P02

最终交流类型：墙报

Revealing the Microscopic Fatigue Mechanism of As2Se3 Ovonic Threshold Switching Selector

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The ovonic threshold switching (OTS) selector is a promising candidate for suppressing leakage currents and providing driving currents in storage arrays. However, its performance falls short of the strict requirements of memory devices due to insufficient research on its mechanism, hindering further improvement. In this study, the traditional binary system As2Se3 is investigated, and electrical and microstructural characterization techniques are employed to study its operating mechanism. During the cycling process, the off-state leakage current gradually increases until failure. By examining the microstructure of the devices at different cycling stages, varying degrees of elemental segregation and TiN diffusion phenomena were observed. These observations provide compelling evidence for device degradation analysis, suggesting that these phenomena are likely associated with the local filament melting mechanism of the device at high temperatures.

D06-P03

最终交流类型：墙报

Study on the phase transition behavior of Ge2Sb2Te5 alloy by indium doping

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Phase change memory (PCM) is a promising storage technology for the next generation non-volatile information storage devices, known for its fast read/write speeds, low operating power consumption, and good CMOS process compatibility. Among which Ge2Sb2Te5 (GST) alloy is the maturest material utilized in PCM, while the relatively low thermal stability inhibits its further applications. In this study, indium doped GST alloy with different concentrations were prepared using magnetron co-sputtering method. The phase transition characteristics at different concentrations were investigated through resistance-temperature (R-T) measurements, X-ray diffraction (XRD) experiment, transmission electron microscopy (TEM) and thermal field simulation using COMSOL software. It was found that indium doping with low concentration can promote the thermal stability of GST alloy, postponed the transition from face-centered cubic (fcc-) to hexagonal (hex-) phase. While a higher indium doping concentration will result in the phase separation phenomenon during the heating process, and the formed InTe nanograins leading to a lower maximum temperature under the same current excitation.

D06-P04

最终交流类型：墙报

Dielectric and Elastic Properties of t-HfO2 Thin Films from First Principles

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Hafnium oxide (HfO2) is regarded as a promising material in the integrated circuit industry, primarily due to its high dielectric constant (k value) and wide bandgap. However, the high-k properties of HfO2 are often present in metastable tetragonal phase, and the mechanisms influencing its dielectric properties remain unclear. In this paper, we investigate the impact of material thickness, lattice distortion, and interfacial stress on the dielectric

properties of t-HfO2 thin films using first-principles calculations. We find that the dielectric constant of t-HfO2 thin films becomes larger with increasing thickness. Meanwhile, specific range of tensile strain can enhance the dielectric constant t-HfO2 thin films. Additionally, the thickness-dependent dielectric constant of t-HfO2 thin films persists under the effect of the interfacial stress from HfO2/ZrO2 interfaces. Finally, we have also studied the distinctive anisotropic behaviors of t-HfO2 thins. Such atomically thin t-HfO2 films exhibit potential for high capacitance, and provide an important path for realizing future high-performance DRAM devices.

D06-P05

最终交流类型：墙报

CMP characteristics of High-K material HfOx thin film with a variety of process parameters

Wei Wang[1], Ming Zeng[1], Libin Jia[1], Weiran Li[1], Hongbo Sun[1], Guilei Wang[1], Chao Zhao*

1. Beijing Superstring Academy of Memory Technology

Hafnium oxide (HfOx) is studied in the field of 3D transistor as a HK material for better insulation and higher current drive capability to improve the performance of nanoscale transistors. CMP process need be applied to fully remove surface HfOx in multilayer film stack structure and achieve the purpose of planarization. As we all know, the CMP characteristics of desired removal rate and within-wafer non-uniformity (WIWNU%) play an important role in CMP process. In this paper, the variation of the removal rate and the non-uniformity for HfOx thin film were studied with various process parameters (such as polishing time, slurry flow rate, head pressure, head and table speed). By the polishing time split test, the result showed that as the polishing time increased, the remove rate also increased and presented a clear linear correlation(R2=0.91), and WIWNU was relatively good at the polishing time of 60s. Slurry flow rate (175,230,300ml/min) split test result showed that the remove rate and the slurry flow rate were strong linear correlation (R2=0.96), and WIWNU got better as the slurry flow rate increased, which could reach 5.2% at 300ml/min. Besides, for head pressure split test (1,2,3.5psi), the remove rate and the head pressure were positive correlation (R2=0.99), and WIWNU performance was better at 2psi. Finally, high head and table speed (100/103rpm) had better WIWNU performance which could improve 34% compared with low head and table speed (87/93rpm), and the remove rate could improve 23%. In general, the removal rate and the non-uniformity of HfOx thin film can be tuned by changing CMP process parameters, which can enhance the confidence about the feasibility of HfOx-CMP in the 3D transistor application of advanced technology.

D06-P06

最终交流类型：墙报

A comparative study of surface treatment methods for SiN/SiO stacked layers after etching in 3D DRAM

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In the 3D DRAM process, dry etching is used to create holes in the O/N layer, followed by the formation of a polysilicon layer at the bottom of each hole and the appearance of a polymer containing O/F on the surface. Various Asher processes and wet clean processes were employed to assess the removal capability of this polymer layer, with TEM and EDS utilized for data analysis. Our study revealed that conventional O2/N2 Asher treatment was unable to completely remove the polymer layer using DSP (Dilute sulfuric acid and hydrogen peroxide), SPM(sulfuric acid hydrogen peroxide mixture), DHF(dilute HF), APM(ammonium hydroxide hydrogen peroxide mixture) or other cleaning solutions (under conditions where SiN/OX layer recess<4nm). Comparative analysis

indicated that the most effective cleaning result was achieved through a combination of DHF+SPM+APM solutions. This approach resulted in weaker "F" and "O" signals at the bottom of each hole. Based on these findings, we optimized our asher process by replacing O2/N2 with an H2/H2 mixed gas scheme and implementing a wet clean method involving DHF_SPM_APM to achieve complete removal of "F" and "O" polymers when SiN/OX layer recess <2nm. We conducted further research on the cleaning protocol and found that the dry etching process would form a polymer at the etching interface of SiN/Poly. This polymer could easily prevent high selectivity isotropic gas etching/wet etching. Based on this discovery, we applied the wet cleaning method to the pretreatment step of SiN or polysilicon etching processes. Introducing this cleaning protocol improved the blocky etching caused by polymer residues and enhanced the uniformity of etching, thereby expanding the process window for gas/wet etching.

D06-P07

最终交流类型：墙报

WET Lateral etching of Si3N4 in 3D DRAM Structures

Chaoyang Guan[1], Mengyuan Zhu[1], Jiao Jin[1], Jiabao Sun[1], Shaohua Wang[1], Huimin Ren[1], Wenjun Chen[1], Jian Liu[1], Baodong Han[1], Zhonghua Jin[1], Chao Tian[1], Libin Jia[1], Hongbo Sun[1], Guilei Wang[1], Chao Zhao*

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3D DRAM (3D Dynamic Random-Access Memory) is an innovative internal technology that increases internal capacity and performance by stacking multiple layers of storage units vertically. For multi-layer stacked structures, the selective definition of film depth cannot be achieved without precise wet lateral etching. The objects of wet etching mainly include silicon oxide (SiO2), silicon nitride (Si3N4), monocrystalline silicon (Si), polycrystalline silicon (Poly), metal films, etc. This paper mainly focuses on the wet lateral etching of silicon nitride, the key parameters of the study mainly include nitride etching length, etching uniformity, etching profile and SiO2 loss. Hot phosphoric acid (H3PO4) has been typically used for the wet etching of Nitride. In order to improve the selectivity of Si3N4 to SiO2, SiO2 etching inhibitors can be added in H3PO4. In this study, HPO3 added with different additives was used for wet lateral etching of Si3N4. The lateral etching length, etching uniformity of Si3N4 and SiO2 loss was analyzed. The loss of additive-A H3PO4 to SiO2 is greater than 3nm, and the selectivity of Si3N4 to SiO2 is less than 200, which cannot meet the process requirement. The additive-B H3PO4 has almost no loss to SiO2, the wet lateral etching length reaches 250nm, and the up/down etch uniformity is less than 1nm, which can meet the initial process requirement. In order to further investigate the stability of 3D DRAM structure, we extend the H3PO4 process time, and when the wet lateral etching length over 400nm, found oxide layer bending and parts of the area have collapsed. In order to address structure stability issue, we added a rapid thermal annealing (RTA) process after Oxide/Nitride stack films dep. Based on the above process conditions, we did different conditions of wet lateral etching nitride lengths by using additive-B H3PO4. The result showed that Oxide/Nitride stack films after RTA process, the etching rate of H3PO4 etching Nitride deceased by 35%, indicating that the density of Nitride films increased. And it was also found that when the Nitride lateral etching length reaches 500nm, the 3D DRAM structure still remains consistent and no collapse occurs. We suspect the possible mechanism is that the RTA process can help remove impurities generated during the growth of oxide and nitride, and after high temperature anneal process, the density of oxide and nitride film quality changes better, helping to improve the stability of the structure. In this work, the effects of different additives of H3PO4 on the nitride wet lateral etching length, the etching uniformity and the SiO2 loss were studied, and the effect of RTA process on the 3D DRAM structure stability was also future studied.

D06-P08

最终交流类型：墙报

High selectivity wet etching in 3D DRAM fabrication

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3D DRAM is one of the breakthrough methods for overcoming the challenges in DRAM technology and is an important development direction for the future memory market. In 3D DRAM, stacking more layers of films (such as Si3N4/SiO2/poly/TiN) is crucial for increasing its storage density. However, as the number of stacked layers increases and the precise requirements for special film layers become necessary, challenges such as poor etching uniformity, low selectivity, incomplete etching, and susceptibility to collapse of exposed film layers have emerged in the wet etching process of 3D DRAM manufacturing, severely affecting electrical performance and practicality of the device.

This study investigates the effect of different chemical etchants and etching processes on the etching of SiO2/poly/TiN multilayer films. By changing the type of etchant, etching time, and optimizing the process by combining wet and dry etching, we achieved excellent etching results in the Si3N4/SiO2/poly/TiN films, resolving the technical deficiencies in the existing etching processes.

Specifically, for the poly lateral etching, ADM (Ammonia Diw Mixture, 90-100s) can reduce phosphorus-doped poly by 12nm. Meanwhile, the etching rate of phosphorus-doped poly in wet etching is faster than that of undoped poly. For the removal of sidewall TiN liner, SPM (Sulfuric acid Peroxide Mixture with WXC-66 additive) fails to remove the TiSiN compound formed at the interface, while APM (Ammonia Peroxide Mixture) exhibits superior cleaning capabilities to TiN and TiSiN. For different multilayer film structures, a combination of wet and dry etching processes effectively solves issues such as residual excess film layers at the bottom and collapse of exposed film layers, achieving high selectivity etching in multilayer films. These results will contribute to exploring solutions to the manufacturing challenges of 3D DRAM.

D06-P09

最终交流类型：墙报

Experimental Study on the Mechanism of Oxide Regeneration in SiN-SiO Stacked Structure

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During the wet etching process of the 3D DRAM's silicon nitride layer, we observed an intriguing phenomenon: the O/N layer of the first pair of silicon nitride layers at the top of the trench can be etched by hot phosphoric acid, while starting from the O/N layer of the second pair, a layer of silicon oxide with a thickness exceeding ten nanometers is generated on the surface layer of silicon nitride. The silicon oxide layer appears to replace the etched silicon nitride in situ. Our analysis suggests that this deposition occurs due to a thin layer of polysilicon on the surface of the silicon nitride, which allows for penetration and dissolution by hot phosphoric acid. Based on the reversible reaction mechanisms between silicate and silica, as well as the reactions between phosphoric acid and Si3N4, we propose a hypothesis regarding the deposition of silica onto Si3N4 surfaces. It is suggested that a thin polycrystalline layer exists on the top surface, which is not completely sealed off. The high-temperature phosphoric acid is capable of dissolving the silicon nitride by penetrating the polycrystalline silicon layer. The resulting accumulation of silicic acid in the sheath layer, due to the inability to promptly remove

its by-product from the solution, leads to a heightened concentration and subsequent precipitation of silica. Characterization of TEM slice morphology and EDS analysis confirmed replacement parts where no nitrogen element signal was detected; morphology remained consistent with original Si3N4 stack without showing typical bone-shaped features after silica deposition.

D06-P10

最终交流类型：墙报

Oxide lateral gas etching uniformity improve in 3D DRAM structure

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In semiconductor processing, high-temperature thin film deposition can lead to metal gate oxidation, significantly affecting the electrical performance of devices. To ensure stable device performance in subsequent processing steps following metal gate formation, it is crucial to strictly control the deposition temperature of thin films below 500°C. However, reducing the deposition temperature may alter the properties of the oxide film, posing challenges for the selective etching of oxide and nitride films in traditional wet etching processes.

To address this issue, plasmaless gaseous etching technology has been introduced. Compared to traditional wet etching methods, gas etching offers a higher selectivity between oxides and nitrides and resolves the issue of differential etching rates of oxides under varying temperatures, making it widely applicable in many planar structures.

Nevertheless, achieving uniformity in the lateral etching of deep holes remains a challenge in 3D DRAM structures. Planar structures typically employ high-temperature, short-duration, and medium-pressure reaction conditions. But in 3D DRAM structure, short gas exposure times lead to inadequate reaction of the bottom oxide with the etching gas in deep hole etching. This disparity in etching rates between the top and bottom surfaces hinders the uniformity required for cross pillar lateral etching.

To tackle this challenge, this study utilized the gaseous etching tool, based on the mechanism of non-plasma gas etching, by increasing pressure and extending the duration of individual reactions, the top and bottom oxide films were brought to a saturation threshold, enhancing the lateral etching uniformity of deep holes. Experimental results demonstrated that the lateral etching uniformity for holes with a depth of 600nm and a width of 45nm was within ±3nm, meeting the current process requirements. The successful application of this method provides an effective solution for addressing the lateral etching uniformity challenge in 3D DRAM structures.

Overall, the use of non-plasma gas etching technology in semiconductor processing has proven to be a valuable solution for lateral etching in deep holes, particularly in 3D DRAM structures. By optimizing reaction conditions and pressure levels, the gaseous etching tool has effectively enhanced the selectivity and uniformity between oxide and nitride film etching, ensuring stable device performance in subsequent processing steps. This study highlights the importance of innovative etching techniques in overcoming challenges related to low-temperature thin film deposition and selective etching processes in semiconductor manufacturing.

D06-P11

最终交流类型：墙报

Radical etching characteristic of titanium nitride using NF3 and hydrogen mixtures on 3D multilayer stack transistor integration

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Titanium nitride (TiN), with excellent electrical and physical properties, is widely used for applications in nanoscale devices, especially for reduce the parasitic capacitance of bit line (BL) and the word line (WL) in DRAM devices. In achieving high aspect ratios 3D structures, it is common practice to use wet lateral etch for removing with homogeneous coverage of sidewalls and bottom TiN formed by atomic layer deposition (ALD) process1,2. However, the unprepared etch profile and worse uniformity directly impact the device performances and lead to slower transfer speeds. Here, we demonstrate a generic way to uniform lateral etch TiN by mixing fluorine-based gas (CF4/NF3) in a conventional ICP plasma etch tool3， in which the tuning gas was excited in a remote plasma source (RPS). The different parameters such as gas flow composition, temperature, bias power and pressure, which are key factors in the control of the TiN etch rate, was examined. Remarkably, by optimizing the radical etch process conditions, selectivity of TiN/OX nearly 600:1 without severe metal profile artifacts is achieved. Our study provides a simple yet approach for TiN lateral etching in high aspect ratio structures, holding great potential in fabricating diverse 3D nanostructures.

D06-P12

最终交流类型：墙报

The feasibility of the radical etching on TiN layers in 3D multilayer stack structure

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In 3D multilayer stack structure, the lateral etching of titanium nitride (TIN) as conductive materials has been attracted more attention in the recent years. Limited by anisotropic characteristic, traditional dry etching is not suitable for TIN lateral etching. Wet etching has been regarded as the promising technology for TIN lateral etching because of its excellent isotropy. However, TIN atomic layer deposition (ALD) has generated the unexpected seam. Wet chemistry tends to etch TIN along the seam, which leads to the poor profile and further degrades the performance of device. Radical etching has been a candidate method for TIN lateral etch due to the high tolerance of seam. In this paper, the radical etching of TIN has been investigated by use of remote plasma. The radicals which are extremely reactive are generated by filtering charged particles (e.g. electrons, ions) in plasma. The profile of TIN by radical etching is better than which is by wet etching. The excellent uniformity of TIN which is TIN etch amount in different layers has been realized by a one-step main etch (ME) step through increasing chamber pressure (5 mtorr→50 mtorr). The increased pressure leads to more radicals in chamber, which can improve the reaction between radicals and bottom TIN. In addition, the radical etching performance of TIN with different critical dimension (CD) has been explored. For the small CD structure (20 nm), the high aspect ratio makes reactions between radicals and bottom TIN more difficult, which promotes the loading effect of TIN uniformity. The breakthrough (BT) step with bias power 50W has been introduced for enlarging incoming CD. The bias power can facilitate the secondary ionization of molecules in chamber, which can generate more ions. The generated ions bombard the surface of TIN, leading to the increased CD. By combining BT with ME step, the excellent uniformity of TIN has been realized in a small CD structure. This work provides a new method for TIN lateral etching in 3D DRAM.

D06-P13

最终交流类型：墙报

SILICON OXIDE/TITANIUM NITRIDE/ SILICON OXIDE/TITANIUM NITRIDE STACK ETCHING

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One of the key technical challenges in 3D device manufacturing is precisely etching holes or trenches in a stack of layers that are vertically arranged by alternating thin films. This work aims at the etching of silicon oxide/titanium nitride/ silicon oxide/titanium nitride (ONON) periodic stack etching through a two-step etching scheme. As is well-known, account of different film layers involving diverse chemical reaction mechanism, the multi-layer stack materials are prone to encounter the wavy sidewall topography, which will make it difficult to effectively fill the holes or trenches and worsen the device electrical performance test results. Herein, by adjusting the cycle mode of RF power, pressure and gas simultaneously, the passivation distribution and ion bombardment intensity on the surface of different film layers were optimized to achieve smooth morphology etching of vertical sidewalls.

D06-P14

最终交流类型：墙报

A Study On Lateral SIN with Radical Etching

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As the traditional planar dynamic random access memory (DRAM) has reached the scaling limit. 3D DRAM has become one of the most promising storage devices to meet the growing demand for large-capacity data storage device. In this work, the lateral etching of silicon nitride (SIN) has been realized by a Radical etcher using NF3/H2/Ar as the etching gases due to the excellent isotropy of radical etching. The etch rate of SIN has been investigated as a function of RF power, working temperature and H2 ratio. It was found that the higher power and temperature offer a high etch rate. For H2 ratio, the generated H radicals can react with F radicals which are the main etchant of SIN. The higher H2 ratio decreases the etch rate of SIN. In this system, Finally through optimized the process parameters, a smooth surface and sidewall with an excellent profile have been achieved.

D06-PO01

最终交流类型：仅发表论文

Identification of different phase structures of hafnium oxide by atomic image simulations

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Hafnium oxide ferroelectric memory offers non-volatility, low power consumption, fast read-write speed, <1 nm scalability, and CMOS compatibility, making it a promising next-generation nonvolatile memory device. However, due to the metastable property of the ferroelectric phase, hafnium oxide thin film prepared by atomic

layer deposition is polycrystalline and contains several crystallographic phases with similar structures. Besides, the orthorhombic phase and tetragonal phase are nearly indistinguishable even using synchrotron radiation X-ray diffraction, challenging its characterization and mechanism study. Therefore, effectively identifying different phase structures is essential for investigating the microscopic structure and ferroelectric performance. In this work, the multi-slice algorithm was utilized to simulate scanning transmission electron microscopy images. For the experimental part, Cs-corrected scanning transmission electron microscopy was employed to acquire high-angle annular dark-field images and annular bright-field images. Based on the results, we proposed that when utilizing specific orientation to distinguish various phases, imaging conditions such as spherical aberration coefficient, tilt angle, film thickness, etc. affect the analysis to some extent. This work lays the foundation for understanding hafnium-based ferroelectric phase structure.

D06-PO02

最终交流类型：仅发表论文

有机物电解氟化机理研究

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电解氟化技术是通过电解含氟化合物产生氟自由基或氟气，进而与有机物发生氟化反应的过程，该技术具有反应条件温和、产物纯度高、环境污染小等优点。电解过程中氟自由基或氟气在电极上生成，通过与有机物的接触，发生氟化反应。电解条件，如电流、电压、电解质种类和浓度及电导助剂等均会影响电解氟化的效率和产物分布，氟自由基或氟气与有机物的反应过程涉及电子转移、化学键断裂和形成等步骤。对不同的有机物，其反应活性和氟化位点会有所差异，从而导致不同的氟化产物和反应路径。

本文旨在探讨有机物的电解氟化过程和机理，为电解氟化技术的发展和应用提供理论依据。

D06-PO03

最终交流类型：仅发表论文

三氟化氮的电解合成、应用领域及其发展前景

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三氟化氮的合成方法有化学合成法和电解合成法，中国、日本、韩国主要采用电解合成法。三氟化氮是一种在微电子工业中应用广泛的特种气体，主要用作等离子蚀刻气体和反应室清洁剂。在半导体芯片、平板屏幕、光伏电池等制造领域发挥着重要作用。三氟化氮在室温下具有化学惰性，在高温下比氟和氧易于操作。与其它含氟电子气体相比，三氟化氮具有反应速度快、效率高等优点，特别是在蚀刻硅材料时，具有较高的蚀刻速度和选择性，且不会在蚀刻对象的表面留下任何残留物，是一种很好的蚀刻剂。

三氟化氮的需求主要来自半导体产业、面板及光伏电池产业，随着全球半导体、面板及光伏电池制造向中国大陆转移，中国大陆成为全球最大的半导体、面板及光伏电池生产地，三氟化氮的市场空间变得更为广阔。本文旨在探讨三氟化氮的电解合成方法、应用领域及其发展前景。

D06-PO04

最终交流类型：仅发表论文

气相色谱法测定高纯三氟化硼中的微量杂质

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本文提出了一种高纯三氟化硼中微量气体杂质的分析方法，采用配备反吹气路的氦离子化检测器的气相色谱仪实现了高纯三氟化硼中微量 H2、N2、O2、CH4、CO 和 CO2 的分离检测。

D06-PO05

最终交流类型：仅发表论文

膜分离、变压吸附及深冷制氮工艺研究

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氮气是无色无味气体，按体积分数计算，氮气约占空气体积的 78%，作为一种惰性气体，广泛应用于电子工业、金属冶炼、化学工业及生活的各个领域。目前，膜分离、变压吸附和深冷分离是工业生产氮气的常用方法，在工艺选择时，需要根据具体的生产需求和经济条件进行权衡。对氮气纯度低、生产规模小的场合，可以选择膜分离、变压吸附工艺，既可以节省投资成本、降低能耗，又可以满足生产要求。而对于氮气要求纯度高、规模大的场合，则选择深冷制氮工艺。本文深入探讨了三种制氮工艺的优缺点。

D06-PO06

最终交流类型：仅发表论文

基于粉末原子层沉积法制备的电泳粒子及其应用性能研究

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彩色电泳显示器件（EPDs）已在工业界和学术界引起了广泛关注。电泳粒子的制备是彩色 EPDs 构建的核心问题之一。粉末原子层沉积（PALD）是一种气相沉积方法，可以在粉体表面沉积具有单原子层级精度的共形薄膜。本文分别以 PALD 法（以 Al(CH3)3 和去离子水为前驱体）和 Al3+溶液法改性活化有机颜料 R170，再通过耦合-聚合物接枝成功制备了红色电泳粒子。分别构建了基于该电泳粒子的红-白双色与黑-白-红三色 EPDs。结果表明，经 PALD 法活化后，在有机颜料表面形成了较为均匀、致密的包覆层，Al 元素质量分数约 6.43%，高于 Al3+溶液法制得的改性体，后者 Al 元素质量分数约为 2.08%。均匀致密的金属氧化物包覆层为优化粒子表面形貌、空间位阻及表面电荷等性质提供了良好的基础。基于 PALD 法得到的电泳粒子在非极性烷烃介质（电泳显示液）中表现出良好的分散稳定性，粒径(D0.5)约 2.02 μm，带电量足够，制得的 EPDs 在 15V 电压驱动下成功实现双色及一定程度的三色显示。该工作为彩色电泳粒子的制备提供了新的解决思路。